MICROCOPY RESOLUTION TEST CHART
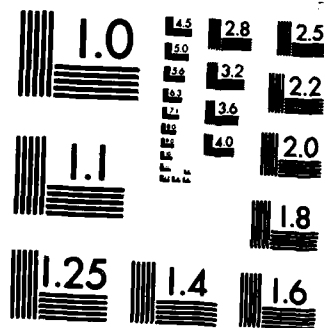NATIONAL BUREAU OF STANDARDS-1963-A

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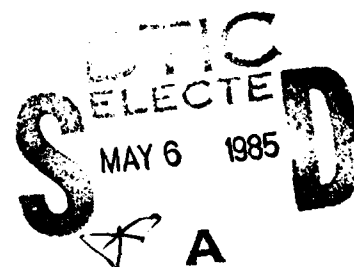# VLSI DEVICE RELIABILITY MODELS

ITT Research Institute

David Coit, William Denson, Kieron Dey, Steven Flint
and Wayne Turkowski

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report details a study in which the objective was to develop failure rate prediction models for VLSI, Hybrid, analog microprocessor, and VHSIC devices. A description is given of the various phases involved in reliability prediction model development, such as; literature collection/review, investigation of failure modes, failure rate data collection, statistical analysis methodologies, model factors quantification, and model validation.

For VLSI, Hybrid and analog microprocessor devices, the models are given in a form which can easily be included in MIL-HDBK-217.

For VHSIC devices, this effort was necessarily limited to the identification of necessary model factors (attributes) which should be included in a quantitative model acceptable for inclusion in MIL-HDBK-217. This effort was necessarily limited to the

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development of a qualitative reliability prediction model due to the lack of available data on VHSIC devices at the time of this study.

PREFACE

This final report for both Phase 1 and Phase 2 was prepared by IIT Research Institute, Chicago, Illinois, for the Rome Air Development Center, Griffiss AFB, New York, under Contract F30602-81-C-0242. The RADC technical monitor for this program was Mr. James Dobson (RBET). This report covers the work performed from October 1981 to May 1984.

The principal investigators for this project was Mr. S.J. Flint and Mr. W.K. Denson with valuable assistance provided by Mr. D.W. Coit, Mr. K. Dey, Mr. W. Turkowski, Mr. J.L. Romeu and Mr. D.E. Rash. Data collection efforts for this program were coordinated by Mr. R. Magoon and Mr. J.P. Carey.

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EVALUATION

The objective of this study was to develop failure rate prediction models for VLSI Devices, Hybrids, Analog Microprocessors, and VHSIC devices. The study met with varying degrees of success. For the VLSI and the Analog Microprocessor parts of the study, the results were very good. For the VHSIC part of the study, inadequate data was available to develop a failure rate model.

Hybrid device field data was available, and a failure rate model for hybrids was developed. However, a review of the model by RADC found that the model was not entirely satisfactory. The present model in MIL-HDBK-217D considers failure contributions for all of the parts in the hybrid package, calculated by using the model in the 217 section covered by each part and then adding them up. The model developed during the contract considered only the failure contributions given by the number of interconnections for the internal parts. In other words, the present model treats the hybrid as a mini-system, (i.e., the failure rate of the particular hybrid is a sum of the failure rates for each of the parts contained inside) while the new model treats the hybrid as a monolithic device. Since the new model did not follow the precedents of MIL-HDBK-217, it was decided that the new model would not be included in the next revision, MIL-HDBK-217E, at least until it can be studied in more detail.

The major significance of the study is that the new models provide a more accurate method of prediction for the particular devices. The models in MIL-HDBK-217D could not achieve accurate results when used for VLSI devices or Analog Microprocessors, and many calls were received on this subject. Also, although a VHSIC failure rate model could not be generated, the study and the report provides a very thorough discussion of the possible failure modes and problems that will be found in the use of VHSIC devices. A quantitative model is provided which identifies factors, attributes and possible failure modes which must be considered.

James J. Dobson

JAMES J. DOBSON
R&M Techniques Section
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Technical Report Summary

As a result of this study, IIT Research Institute has developed a new failure rate prediction model for VLSI devices and analog microprocessors which addresses current state-of-the-art microcircuits. Also, revised failure rate prediction models have been developed for hybrid microcircuits. All models have been formatted for easy inclusion into a future revision of MIL-HDBK-217.

A preliminary model form has been developed for failure rate prediction of VHSIC devices. However, due to the fact that no empirical failure rate data was available on this emerging technology at the time of this study, it was not possible to establish quantitative model factors.

The proposed prediction methodology affords the optimal consideration of those qualities common to practical reliability assessment techniques. These desirable characteristics include:

o   Reasonable accuracy over the total range of all parameters considered in the technique.

o   A relatively uncomplicated approach which is easy to use.

o   A dynamic, flexible expression which, through simple modification, allows for evaluation of newly emerging technology.

o   Appropriate discrimination against design and usage attributes which contribute to known failure mechanisms.

The prediction methodology provides the ability to predict the total reliability as a function of the characteristics of each device, the technology employed in producing that device, and those external factors, e.g., environmental stresses, which have a significant effect on device reliability.

In formulating the proposed technical approach, it was essential to identify the various factors associated with each of the microelectronic

iii

devices considered in this study which will ultimately impact on their reliability. These variables, which must be considered in detail, include:

o Function

o Technology

- Fabrication techniques
- Fabrication process maturity
- Failure mode/mechanism experience
- Degree of similarity with existing technology

o Complexity

o Packaging considerations

o Effectiveness of screening and test techniques

o Operating temperature and environment

o Application considerations

The development of a prediction model requires an evaluation of the contribution of each of these critical factors, and the integration of their collective effects into a manageable procedure that can be applied by reliability engineers using information normally available during the equipment design phase.

The approach IITRI used for this study combined considerations from each of the methods described above. It employed model(s) based on failure mode/mechanism knowledge to establish the fundamental reliability relationships, the statistical analysis of existing accelerated life test results to determine the impact of various reliability attributes, and the utilization of field experience data to scale and verify the relationships. This approach involved several study tasks. These tasks included: 1) a literature review to define the attributes of devices which will be considered in the study; 2) development of a theoretical model to identify data needs; 3) data collection; 4) data reduction and

analysis; 5) development of a preliminary semi-empirical model; and, 6) model refinement and verification.

It is recommended that the models developed as a result of this study be adopted in a future revision of MIL-HDBK-217. It is believed that these models represent a reasonable and accurate analysis of the reliability performance of VLSI logic, Analog Microprocessor and hybrid microcircuits in actual field usage conditions. It is further believed that these models represent a substantial improvement over the existing models in MIL-HDBK-217.

It is also recommended that RADC continue to study the reliability of VLSI devices over the next few years. This study was based on the necessarily sparse data accumulated during the first few years of VLSI technology. While statistically inconclusive, evidence was uncovered during the course of this study which would indicate a substantial reliability improvement in VLSI devices from 1977 to 1981 - perhaps as much as a factor of 5 improvement. For this reason it is important that the reliability of these devices be tracked over the next few years until such time as they may be regarded as a mature and stable product.

It is recommended that RADC support an effort dedicated solely to the collection and analysis of failure rate data on microwave hybrids. These hybrids represent a significant departure in technology from the conventional hybrid, and high-quality data on these devices is simply not available at the present time.

It is also recommended that RADC pursue an effort devoted to the collection and analysis of reliability data of analog microprocessors and VHSIC devices as they mature technologically. This is especially important for VHSIC devices so that the failure rate prediction model presented in this report can be quantified.

Finally, it is suggested that the USAF and RADC closely scrutinize their maintenance data collection and reporting systems. Close coordination of the data needs of the reliability world with the types of information tracked and collected by the logistics world stands to reap tremendous benefits for both parties. A good deal of the time and effort invested in reliability programs is now lost due to inadequate or incomplete documentation. It must be impressed upon program management and technical personnel that a complete, effective reliability program must include a validation and documentation phase. Documentation, preferably in the form of standard data items (DID's), must be made available to the DoD community if others are to benefit from the acquired knowledge and lessons learned.

It is concluded that the proposed failure rate prediction models for VLSI, hybrid microcircuits and analog microprocessors represent accurate, technically sound models for the evaluation of anticipated field reliability performance for these devices.

It is also concluded that these models represent a substantial improvement over the existing models. For this reason it is proposed that these models be incorporated into a future revision of MIL-HDBK-217.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

TABLE OF CONTENTS (CONT'D)

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES (CONT'D)

LIST OF TABLES (CONT'D)

LIST OF TABLES (CONT'D)

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1.0 INTRODUCTION

IIT Research Institute is pleased to submit this Final Technical Report for Phase 1 and Phase 2 of Air Force contract F30602-81-C-0242, "VLSI Device Reliability Models". Phase 1 of this contract accomplished an in-depth analysis of the reliability of VLSI microcircuits and hybrid devices and Phase 2, VHSIC microcircuits and analog microprocessors. New and/or revised failure rate prediction models have been developed and formatted for inclusion into a future revision of MIL-HDBK-217.

Failure rate and mean-time-between-failure prediction capabilities are essential tools in the development and maintenance of reliable electronic equipments. Predictions performed during the design phase yield early estimates of the anticipated equipment reliability, which provide a quantitative basis for performing proposal evaluations, design trade-off analyses, reliability growth monitoring, the life-cycle cost studies.

The advancement of new technologies and techniques as well as an improved understanding of the complexities of environmental and operational factors require that either new or updated models be developed to insure reasonably accurate reliability predictions.

1.1 Objective

As a result of this study, IIT Research Institute has developed a new failure rate prediction model for VLSI devices and analog microprocessors which address current state-of-the-art microcircuits. Also, revised failure rate prediction models have been developed for hybrid microcircuits. All three models have been formatted for easy inclusion into a future revision of MIL-HDBK-217, and are included in this report as Appendix A.

For VHSIC devices, this effort was necessarily limited to the identification of necessary model factors (attributes) which should be

1-1

included in a quantitative model acceptable for inclusion in MIL-HDBK-217. This effort was necessarily limited to the development of a qualitative reliability prediction model due to the lack of available data on VHSIC devices. As of yet, none of the VHSIC prime contractors have a finalized version of a VHSIC chip. Since any reliability prediction model included in MIL-HDBK-217 will have to be validated from empirical reliability data, the development of a quantitative model is not possible until empirical data is available.

The proposed prediction methodology affords the optimal consideration of those qualities common to practical reliability assessment techniques. These desirable characteristics include:

o   Reasonable accuracy over the total range of all parameters considered in the technique.

o   A relatively uncomplicated approach which is easy to use.

o   A dynamic, flexible expression which, through simple modification, allows for evaluation of newly emerging technology.

o   Appropriate discrimination against design and usage attributes which contribute to known failure mechanisms.

The prediction methodology provides the ability to predict the total reliability as a function of the characteristics of each device, the technology employed in producing that device, and those external factors (e.g., environmental stresses) which have a significant effect on device reliability.

2.0 RELIABILITY PREDICTION MODELING TOOLS & TECHNIQUES

In full compliance with the Statement of Work, IITRI has pursued a program of data collection, study, and analysis culminating in the development of the prescribed reliability prediction models. This approach emphasized statistical analysis of empirical field-use data such that the models will, in fact, predict reliability in all military environments. IITRI preceded the field data collection/analysis effort with an analysis based on accumulated reliability experience data and information. The functional and physical attributes and failure mechanisms suggesting significant reliability relationships provided a firm physical foundation for model development. Analysis of this information also allowed for the development of accurate, logical models without the luxury of an extremely large database.

Vendor and equipment data were used, but strong emphasis was placed on use of field operation data. When the data for any device type proved to be limited and inadequate to support the development of the required models, an alternative approach was pursued. This alternative approach consisted of the development of models based on theoretical considerations and tested with the limited data available.

2.1 Modeling Approach Overview

In formulating the proposed technical approach, it was essential to identify the various factors associated with each of the microelectronic devices considered in this study which will ultimately impact on their reliability. These variables, which must be considered in detail, include:

o Function

o Technology

    - Fabrication techniques
    - Fabrication process maturity

- Failure mode/mechanism experience
- Degree of similarity with existing technology

o   Complexity

o   Packaging considerations

o   Effectiveness of screening and test techniques

o   Operating temperature and environment

o   Application considerations

The development of a prediction model requires an evaluation of the contribution of each of these critical factors, and the integration of their collective effects into a manageable procedure that can be applied by reliability engineers using information normally available during the equipment design phase.

The underlying problem of model development centers around the acquisition of representative data in order to assess the effects and interrelationships of the various factors and parameters. Several possible approaches were suggested, each of which has definite merit, but is also subject to limiting constraints. The approach employed by IITRI endeavored to utilize the collective data and knowledge offered by the several approaches, and subject it to careful, analytical scrutiny to censor out conflicting and discrepant information.

One readily obvious approach for deriving the necessary data would be the analysis of accelerated life test results. This presupposes that a large number of each of the device types had been tested, or are currently being tested, in various combinations representing the technologies, processes, etc. The results of such controlled tests did provide some indication of the characteristics and peculiarities of those devices as a function of the several configurations, stresses, and applications included in the test design. However, the extrapolation of these accelerated test results to more normal conditions was open to questions of validity due to uncertainties regarding the extrapolation algorithm.

2-2

Further, while test data under controlled accelerated conditions should aid in understanding the reliability characteristics, presently available data does not sufficiently cover the wide range of technologies and stress conditions that would be necessary in order to place major dependent on this approach alone.

An alternate approach involved the development of reliability model parameters based on a knowledge of fabrication techniques and the anticipated failure modes. Also required by this approach was a thorough understanding of the fundamental physical-metallurgical-chemical-electrical degradation mechanisms involved, as well as the proportionate weighting of these mechanisms in translating to the various configurations each of the devices assumed.

A third approach relied solely on the collection and reduction of empirical field data where the pertinent information with respect to the model parameters was extracted using suitable statistical analysis techniques. This approach provided optimal applicability since the field data reflected the actual reliability experience of the devices operating in their use environment. However, it required the collection and reduction of a large database on the entire range of device configurations and application environments in order to evaluate each of the critical factors. In some cases, particularly with new devices, the amount of data needed to be statistically significant was not available.

Since most of the devices to be studied are either very new or are "custom" devices, and, as such, are low-population low usage parts, the development of statistically large databases was impossible for these devices.

The approach IITRI used for this study combined considerations from each of the methods described above. It employed model(s) based on failure mode/mechanism knowledge to establish the fundamental reliability relationships, the statistical analysis of existing accelerated life test

results to determine the impact of various reliability attributes, and the utilization of field experience data to scale and verify the relationships. This approach involved several study tasks. These tasks included: 1) a literature review to define the attributes of devices which will be considered in the study; 2) development of a theoretical model to identify data needs; 3) data collection; 4) data reduction and analysis; 5) development of a preliminary semi-empirical model; and, 6) model refinement and verification. Figure 2.1 presents a flow chart summarizing the model development program employed in this contract.

2.1.1 Literature Search

A comprehensive literature review was performed for the four device types of this study. The purpose of the literature review was to identify all published information which was thought to be relevant to the reliability of these devices. Literature sources searched included the Reliability Analysis Center (RAC) automated library information retrieval system, the *Defense Technical Information Center* (DTIC), the Government Industry Data Exchange Program (GIDEP), and the RADC technical library. Additionally, manufacturers and researchers of these device types were queried to obtain relevant information.

The primary objective of the literature review was to locate references whose content could be used to define relevant device characteristics and to hypothesize a model form, to supplement the data analysis process, and to provide the proposed reliability prediction models with a sound theoretical foundation. Of the documents initially identified, those found to be relevant are listed in the References section of this technical report.

Particular emphasis was placed on the literature search task because of anticipated shortages of reliability data. To insure a thorough and extensive literature search, a five part search methodology was determined
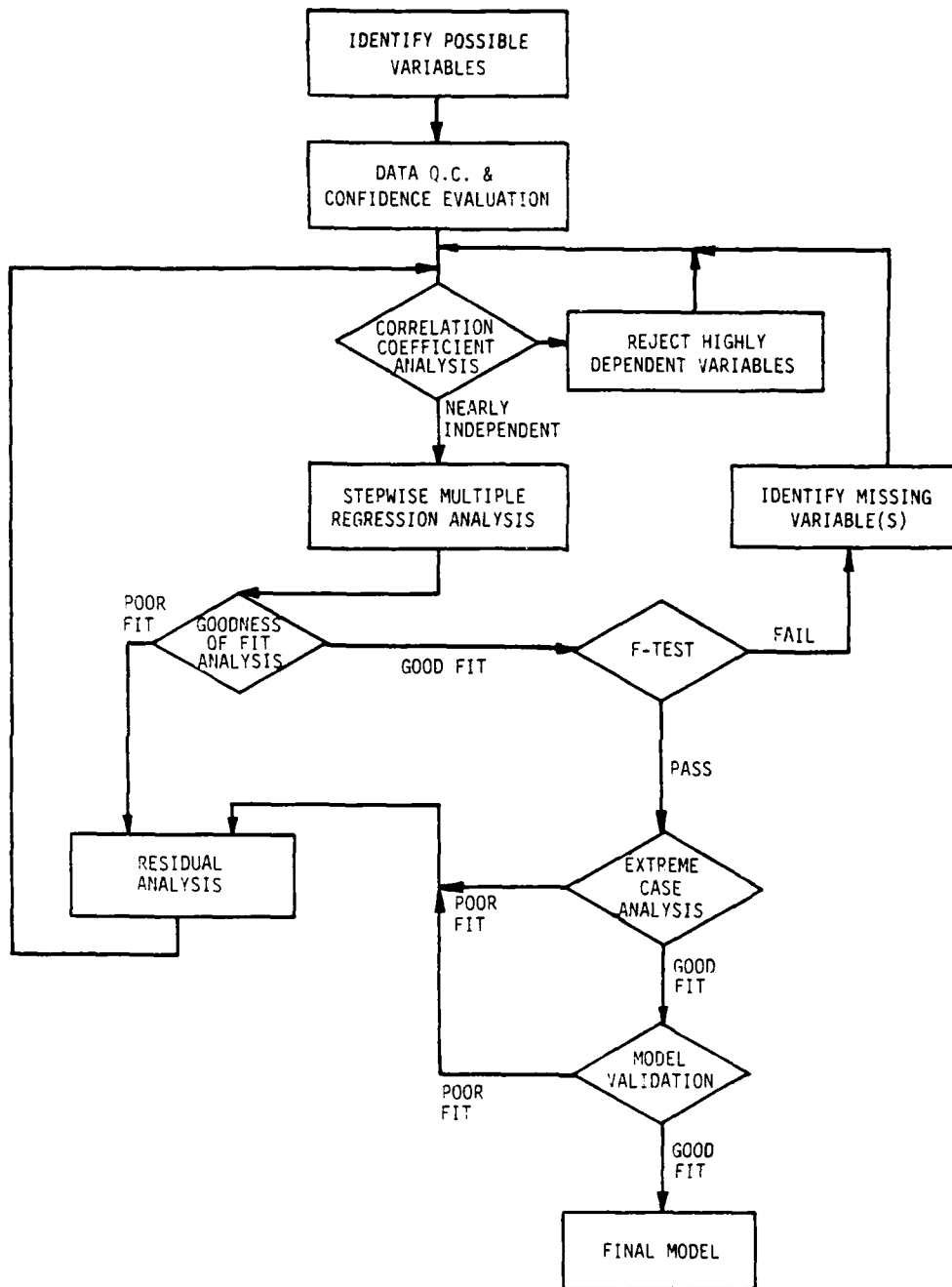
FIGURE 2.1: FLOW CHART OF MODEL DEVELOPMENT EFFORT

before initiation of the search. The five part search methodology is presented in Table 2.1.

In the problem/goal definition step, IITRI engineers and information specialists defined the key concepts relative to these four device types reliability, and also identified related areas which could potentially yield pertinent information. These concepts and related areas are discussed in detail in the devices respective sections. Other factors which were considered at this stage included the time span available for the search, and its general scope.

TABLE 2.1: LITERATURE SEARCH AND REVIEW METHODOLOGY

Subtask No.	Description
1	Problem/Goal Definition
2	Information Resource Identification
3	Literature Search
4	Literature Survey
5	Information Evaluation

The primary activity in the information resource identification step consisted of identifying potential sources of relevant abstracts, indexes, reference works, and technical journals which were applicable to the problems defined in the previous step. As stated before, the RAC automated library system, DTIC, GIDEP and the RADC technical library were identified as appropriate information sources.

Subtask number 3, the literature search was performed using the key concepts defined in the first step and the information sources identified in the second step. The literature search step consisted of identifying and obtaining relevant documents. Both manual and automated search methods were used.

The literature survey and evaluation steps (subtasks 4 and 5) were the most important aspects of the literature search and review process. The literature survey step consisted of extracting pertinent information from the documents and technical articles. The evaluation step consisted of carefully scrutinizing the information to ascertain whether the information was applicable to this study.

2.1.2 Development of Theoretical Models

A series of reliability models were hypothesized in order to provide some overall direction to this model development effort, and, in particular, to provide background and insight necessary for a productive data collection program. These models were intended for discussion purposes only, yet provided considerable insight into problems which had to be addressed. In the final analysis, the following parameters were deemed important to any reliability model for VLSI devices:

- o Implementation Technology
- o Device Complexity
- o Packaging Technique
- o Application Evironment
- o Quality Level
- o Operating Temperature
- o Device Function (memory, logic, etc.)

For hybrid devices, the following parameters were hypothesized as being significant:

- o Packaging Techniques
- o Operating Temperature
- o Device Complexity
- o Application Environment
- o Quality Level

The above parameters were used to guide the data collection activity in their subsequent efforts. The validity of these parameters as useful indicators of reliability will be discussed later in this report.

2.1.3 Data Collection

2.1.3.1 Phase 1 VLSI and Hybrid Mircrocircuits

An extensive data collectior. program was undertaken to collect up-to-date, accurate data to support this modeling effort. In total, 174 hybrid/VLSI vendors were contacted for data via letter request. (Approximately 200 letters were sent, as additional letters were required due to vendor personnel changes, referrals, etc.).

Also, approximately 75-100 telephone calls were made for follow-up action, additional information, new contacts, etc.

Of the 174 initial requests, responses were as follows:

110 No response
 15 Negative reply - No data available
 18 Promised data at later date when available
 26 Sent data
  5 Have data, will not release (proprietary)

The following companies submitted data

1 Advanced Micro Devices
2 Analog Devices
3 Circuit Technology (CTI)
4 Datel-Intersil
5 Fairchild
6 Goddard Space Flight Center
7 Hughes

8   Hybrid Systems

9   Hycomp, Inc.

10 Intel (California)

11 Intel (Chandler, AZ)

12 Interdesign

13 Intersil

14 ITT Microsystems

15 Jet Propulsion Labs

16 Monolithic Memories

17 Mostek

18 Motorola

19 National Semiconductor

20 Nitron

21 Raytheon

22 Sprague

23 Synertek

24 Teledyne Crystalonics

25 TRW Semiconductor

26 Zilog

The following companies refused to submit data due to proprietary interests:

1   Honeywell

2   Integrated Circuits

3   LSI Logic

4   Martin-Marietta

5   RCA Solid State

In addition, the following hybrid/VLSI vendors were contacted directly by IITRI personnel in the course of our data collection effort:

Honeywell - Clearwater, FL   Compugraphic - Wilmington, MA

Martin Marietta - Orlando, FL   Unitrode - Watertown, MA

Harris Corporation - Melbourne, FL   Analog Devices - Wilmington, MA

Motorola - Plantation, FL   Teledyne Crystalonics -

IIT Microsystems - Deerfield   Cambridge, MA

  Beach, FL   Raytheon - Andover, MA

Sprague Electric - Worcester, MA   Exxar - Sunnyvale, CA

Teledyne Philbrick - Dedham, MA   Zilog - Cupertino, CA

Hybrid Systems - Billerica, MA   Signetics - Sunnyvale, CA

Hycomp, Inc. - Sudbury, MA   Teledyne - Mt. View, CA

Datel-Intersil - Mansfield, MA   Siemens/Litronix - Cupertino,
                                            CA

A detailed list of vendors contacted and the results of the contact are presented as Appendix C to this report.

In addition to vendors, a considerable amount of data was received on fielded equipments containing hybrid and/or VLSI microcircuits. A list of the equipments for which data was available is contained in Table 2.2.

TABLE 2.2: EQUIPMENTS FOR WHICH FIELD DATA WAS RECEIVED

Equipment

AN/APN-209	AN/SPS-52(B)	AN/APG-63
AN/APS-52(B)	AN/SPY-1	AN/APG-64
AN/BQQ-5	AN/TSC-60 VI	AN/FPS-108
AN/BRD-7	AN/TSQ-73	AN/ASH-28
AN/FPS-108	AN/USC-26	AN/ASK-6
AN/GKC-1	AN/ARN-131	AN/ASN-108
AN/GYQ-18	AN/AWG-9	AN/ASW-38

Table 2.3 represents a summary of the data accumulated in support of this modeling effort.

TABLE 2.3:   DATA SUMMARY BY PART HOURS

VLSI LOGIC

Environment	Screen Class	Part Hours	Failures
Ground	B	13,680	0
	D	1,756,675,536	171
	D-1	523,697,600	388

VLSI MEMORY

Environment	Screen Class	Part Hours	Failures
Ground	B	37,160	0
	D	172,900,000	38
	D-1	706,376,450	97
Airborne	B	29,551	0

HYBRIDS

Environment	Screen Class	Part Hours	Failures
Airborne	S	96,800,049	101
	B	40,357,993	6
	C	48,384,000	1
	D	730,207,907	299
Ground	S	12,556,276	3
	B	144,778,462	88
	D	135,389,453	174
	D-1	993,189	1
Naval	S	103,048,960	31
	D	9,393,344	0

2.1.3.2 Phase 2 VHSIC and Analog Microprocessors

Both VHSIC devices and analog microprocessors are representative of emerging technologies and low population part types. Therefore, modeling approaches based solely on observed field data were not feasible. In fact, VHSIC devices have not been included in the design of any fielded military equipments. Therefore, alternate data collection and modeling approaches were developed. This section presents in detail the information collection procedure and the preliminary analyses used to develop a useful data/information databank.

The Reliability Analysis Center operated by the IIT Research Institute at Griffiss Air Force Base was solicited to aid in the data/information collection process. The Reliability Analysis Center regularly pursues the collection of parts reliability data including digital, linear/interface, memory/LSI and hybrid microcircuits. Data resources for analog microprocessors which had been collected and summarized prior to the initiation of this study were available for analysis. However, the requirements for extensive data/information resources and the relative lack of available information necessitated additional data collection activities to supplement the existing information.

The data collection activities for VHSIC and analog microprocessors were necessarily different due to their respective stages of development. The following two sections describe these data collection activities.

There are presently no fielded equipments designed with VHSIC devices. Therefore the collection of field experience data could not be considered and alternate data/information approaches were developed. Collection of VHSIC life test data was also impossible because the state of development has not advanced to the point where VHSIC devices can be life tested. It is anticipated that life test data will become available by the end of 1984 for preliminary VHSIC designs. Therefore, the data/information task for VHSIC devices was oriented towards identifying and surveying VHSIC

device designers and experts to obtain information which could be used to hypothesize a failure rate prediction model form.

IITRI has also utilized Reliability Analysis Center services in an attempt to organize a VHSIC reliability workshop so that personnel cognizant of VHSIC reliability factors could meet and exchange information. A letter requesting permission to organize such a workshop was sent to the VHSIC program office, and the subject taken up at the May 11, 1983 VHSIC Steering Committee meeting. It was decided at that meeting that a workshop devoted to VHSIC reliability was premature and hence permission was not granted.

An alternate information collection strategy was developed. A total of 196 VHSIC device experts and designers were identified at 62 industrial and government organizations. Each device expert was sent a survey form which asked, (1) to what extent are you involved in VHSIC reliability?, (2) if you are involved in VHSIC reliability, are you willing to discuss this subject?, and (3) if you are not involved in this subject, can you supply the name and phone number of someone at your facility who is? A complete list of the organizations contacted is included as Appendix D of this report. A total of 47 completed survey forms were returned. Twenty-six of these 47 survey forms were considered positive responses which could potentially yield useful information. Table 2.4 presents a list of those organizations which provided inputs to this study effort. Telephone contacts were then made with individuals at each of these organizations to ask more detailed questions regarding VHSIC reliability. To supplement these activities, information collection trips were made to Hughes Aircraft Co., El Segundo, CA; TRW, Inc., Redondo Beach, CA, and Honeywell, Inc., Minneapolis, MN. IITRI was able to develop a comprehensive databank of VHSIC reliability information as a result of the expert opinion survey, telephone contacts and the three information collection trips.

TABLE 2.4:   VHSIC RELIABILITY SURVEY POSITIVE RESPONSES

University of Illinois
Naval Weapons Center
Honeywell
Raytheon
IBM
Naval Electronic Systems Command
SRI International
Naval Sea Systems Command
ERADCOM
Hughes
Sanders Associates
Naval Avionics Center
Hewlett Packard
Naval Surface Weapons Center
Naval Oceans Systems Center
RADC/ESE
AFWAL
Research Triangle Institute
University of Southern California
Perkin Elmer

Attempts to collect field experience data for analog microprocessors proved to be futile. Because of their low volume usage and recent availability, meaningful amounts of field data have not been accumulated. Therefore the data collection activities for analog microprocessors were concentrated on collecting life test data.

Initially a review of all available analog microprocessors was completed. A list of analog microprocessors is presented in Table 2.5. Included in Table 2.5 are 4-bit microprocessors, 8-bit microprocessors and signal processors.

TABLE 2.5: ANALOG MICROPROCESSOR LIST

Part Number	Description	Technology	Manufacturer
TMS 2100	4-bit microprocessor	PMOS	TI
TMS 2170	4-bit microprocessor	PMOS	TI
TMS 2300	4-bit microprocessor	PMOS	TI
TMS 2370	4-bit microprocessor	PMOS	TI
TMS 2400	4-bit microprocessor	PMOS	TI
TMS 2470	4-bit microprocessor	PMOS	TI
TMS 2600	4-bit microprocessor	PMOS	TI
TMS 2670	4-bit microprocessor	PMOS	TI
HD 4470	4-bit microprocessor	CMOS	Hitachi
MB 88411	4-bit microprocessor	NMOS	Fujitsu
MB 88413	4-bit microprocessor	NMOS	Fujitsu
MB 88535	4-bit microprocessor	CMOS	Fujitsu
MB 88536	4-bit microprocessor	CMOS	Fujitsu
S2200	8-bit microprocessor	NMOS	AMI
S2210	8-bit microprocessor	CMOS	AMI
S2220	8-bit microprocessor	NMOS	AMI
S2400	8-bit microprocessor	NMOS	AMI
HD63L05	8-bit microprocessor	CMOS	Hitachi
HD6805W0	8-bit microprocessor	NMOS	Hitachi
MC6805R2	8-bit microprocessor	NMOS	Motorola
MC6805R3	8-bit microprocessor	NMOS	Motorola
8022	8-bit microprocessor	NMOS	Intel
μPD 8022	8-bit microprocessor	NMOS	NEC
MC68705R3	8-bit microprocessor	NMOS	Motorola
2920	Signal Processor	NMOS	Intel
2921	Signal Processor	NMOS	Intel

The seven analog microprocessor manufacturers represented in Table 2.5 were contacted to request life test, environmental test and/or burn-in data. A total of twelve data records were collected. The merged data consisted of eight observed failures in 3.308×10^6 part hours. Each part was tested at 125°C. A summary of the collected data is presented in Table 2.6.

TABLE 2.6: ANALOG MICROPROCESSOR FAILURE RATE DATA

Data Entry No.	Part Number	Failures	Part Hours	# Parts	Data Type	Temp. (°C)
1	TMS 2100	0	131,000	131	life test	125
2	TMS 2300	0	131,000	131	life test	125
3	TMS 2400	0	132,000	132	life test	125
4	TMS 2600	0	132,000	132	life test	125
5	MC6805R2	1	171,520	171	life test	125
6	MC6805R3	2	8,640	180	burn-in	125
7	MC6805R3	0	100,804	187	life test	125
8	MC68705R3	0	22,680	45	life test	125
9	2920	2	54,336	1,132	burn-in	125
10	2920	1	1,052,748	1,053	life test	125
11	2921	0	43,200	900	burn-in	125
12	2921	2	1,328,208	898	life test	125

Failures which occurred during burn-in testing are generally believed to be infant mortality failures. Indeed, the purpose of "burning-in" microcircuits is to eliminate inherently weak devices which are not representative of the total population. Therefore, failure rates calculated from only burn-in data (data entries 6, 9 and 11) were considered suspect. These data entries would have been rejected from the analysis except for the scarcity of accurate data. However, it was necessary to include these data entries with several restrictions. The failure rates computed from these data entries were considered to be an upper limit and not an accurate measure of the inherent device failure rate.

2.1.3.3 The Nature of the Data

Data collection for this study effort is of two major classes: vendor life test data and equipment level field data which has been tracked back to the part level by use of parts lists, T.O.'s, etc.

Life Test Data

Life test data is typically of high statistical quality--indeed these tests are often designed around statistical theory. In spite of this, the data is of limited value in the derivation of suitable reliability prediction models for two reasons. First, the vendor uses accelerated testing in order to achieve the throughput necessary in a production environment. Typically, temperature and voltage will be the only stresses to which a component will be subjected. This contrasts sharply with typical field usage where the component is installed in an equipment which is subjected to temperature, voltage, shock, vibration, power cycling, humidity, etc. Since these conditions vary from application to application, there is no clear-cut algorithm for extrapolating vendor life test results to actual field usage conditions. The second problem is simply one of credibility: "how much confidence can be placed on data generated by the company which makes the part?". While most vendors are reasonably honest, it stands to reason that they are going to present the quality of their parts in the best possible light. As a result, vendor data is usually used to define the optimistic upper bound on the reliability of the part.

Field Data

Field usage data is theoretically the "ideal" data source, since it represents the actual parts of interest operating in their actual end-use environment. To date, however, it has been impossible to realize the full potential of this data source due to a number of limitations in the data collection process. These can be broadly categorized as data quantity limitations and data quality limitations. Each will be discussed in some depth in the following paragraphs.

o   Data Quantity Limitations

As the discipline of reliability engineering matures, and as reliability engineers become more sophisticated, we realize that there are numerous parameters in the end use environment which will impact the reliability of electronic components. Further, as the number of independent parameters increases, so must the size of the database required to derive a statistically significant model.

Another factor forcing the size of the database to be large is the reliability of present day semiconductors; for a good statistical model it is necessary that the total number of operating hours be large in comparison to the MTBF of the parts being studied. Thus as the reliability of these parts increases, the size of the database must also increase if the same level of confidence is to be maintained in the statistical model derived from this database.

While the above-named forces are driving up the desired size of databases required for sound statistical modeling, there are other forces which are driving down the amount of available data, particularly in military systems.

As integrated circuit technology moves into the domain of VLSI, fewer and fewer piece parts are required to implement a given function. As the number of parts decreases, so does the potential size of the database. Whereas there may be 20-30 5400 series NAND gates in a particular equipment, the use of more than one microprocessor is rare; thus, for this equipment, 1000 hours of operating experience will generate 20,000 - 30,000 hours of NAND gate reliability data, but only 1000 hours of microprocessor reliability data. Further, it makes good sense to merge NAND gate data with that of AND gates, OR gates, NOR gates, etc. due to commonality of design, complexity and stress. It is very difficult to merge data on the uP with that of any other part. As a rule, the quantity

of data available on a part type or part class appears to be inversely related to the complexity or sophistication of the part class.

An additional limitation on the quantity of data available for military systems is due to the nature of DoD equipments. They are procured to long lead times, in small quantities and are deployed with relatively low utilization ratios (i.e. the ratio of operating time to non-operating time). In a typical fighter aircraft for example, the utilization ratio is about 0.04. It therefore requires 25 years of deployment ($\frac{1}{0.04}$) to accumulate 1 years worth of operating time. (The authors realize that the reliability effects of non-operating periods are not accounted for by this analysis). As such, for low usage parts, the entire population of fighter aircraft in the USAF may only accumulate a few hundred thousand operating hours per year on a part that only fails once every 10,000,000 hours. Clearly it is very difficult to collect statistically significant amounts of data under such circumstances.

o   Data Quality Limitations

As previously mentioned, data collected in support of this study was of two major types, vendor life test data and actual field experience data. Vendor data is typically of very high quality, but low utility, where a field experience data is of relatively poor quality, although its utility is potentially very high.

Life test data, as with most laboratory test data, is of high quality. Test conditions are tightly controlled and the tests are designed to produce statistically significant results. The problem with this testing is that it is not particularly representative of field usage conditions. Life test data is particularly useful for quantifying the effects of temperature on reliability, but is of limited use in predicting field usage reliability due to the lack of stresses other than temperature and voltage.

2-19

Field usage data is potentially the most desirable of all since it represents the actual reliability of the part in its actual end-use environment. This potential is rarely achieved, however, due to the cost of keeping detailed records on operating time, failure events, etc.

A major source of data for military equipments is the maintenance data systems, of which there are several (USAF AFM66-1, NAVY 3-M, etc.). These systems are designed to provide equipment-level statistics such as availability, MTTR, MTBF, MTBMA, etc. Some also provide information on failed components in order to assist in spares provisioning and logistics support. None of these systems has attempted to track reliability to the piece-part level. We have found, however, that this can be done with some degree of accuracy, by using failure records from the maintenance data system in conjunction with a parts list for the equipment and a summary of equipment operating times (the latter of which must be obtained from other sources).

There are problems with this technique. Parts lists are "living documents": engineering changes and design modifications are common throughout the life-cycle of the equipment. In a mature system, it is conceivable that in an entire population of equipments of a given nomenclature, no two will be exactly alike. As a result, the specific parts list or T.O. which is used is only approximately correct--minor variations may be found from equipment to equipment. These minor differences can result in "noisy" data. For example an erroneous parts counts will cause the estimated failure rate to be higher or lower than it should actually be.

Operating hours also cause errors and "noise" in the data. For military systems, operating hours are usually supplied in the form of hours per month for a specific equipment. In truth this number represents the mean of the (approximately normal) distribution of operating hours of all equipments of a specific type over the required time period. Again

2-20

errors may be expected to the degree that the actual operating times vary from the mean.

One of the major problems with military data systems is the lack of continuity of the data. It is virtually impossible to track an equipment from "cradle to grave". At best, it is possible to monitor the equipment population during certain "windows" during the life-cycle. Consider for example, the situation in Figure 2.2. These equipments were arbitrarily chosen to exhibit a lognormal distribution of failures. If we were to gather data during the window defined by calendar year 1980, the data would show that in a population of these equipments there were 6 failures during 1980. From other sources, we could determine that this particular equipment operated 46 hours per month, or 552 hours per year. If we assume the failures to be exponentially distributed, we would then expect this equipment to have a mean time between failures (MTBF) of $\frac{552}{6}$ or 92 hours. Also, based on the data available in the "window", we might assume that equipment #3 has an MTBF significantly different from the others. One may then study the data further in an attempt to discover why this is so.

If in fact all the data on these equipments was available, it could be determined that each equipment is exhibiting failures which are log normally distributed in time, and that each of the equipments observed is at a different point in its life-cycle.

Much of the military data used in this study was collected by aggregating the failure information from a number of such windows. Studies of the time dependance of failure rate are clearly futile for such data, since time "zero" represents only the beginning of the window and has no absolute meaning. Theory would indicate that for a large number of equipments at random points in their life-cycle, the hazard rate within any window would be constant - the same result as would be realized if data were collected on each equipment from actual time zero and the failures were exponentially distributed. In other words, failure data

2-21
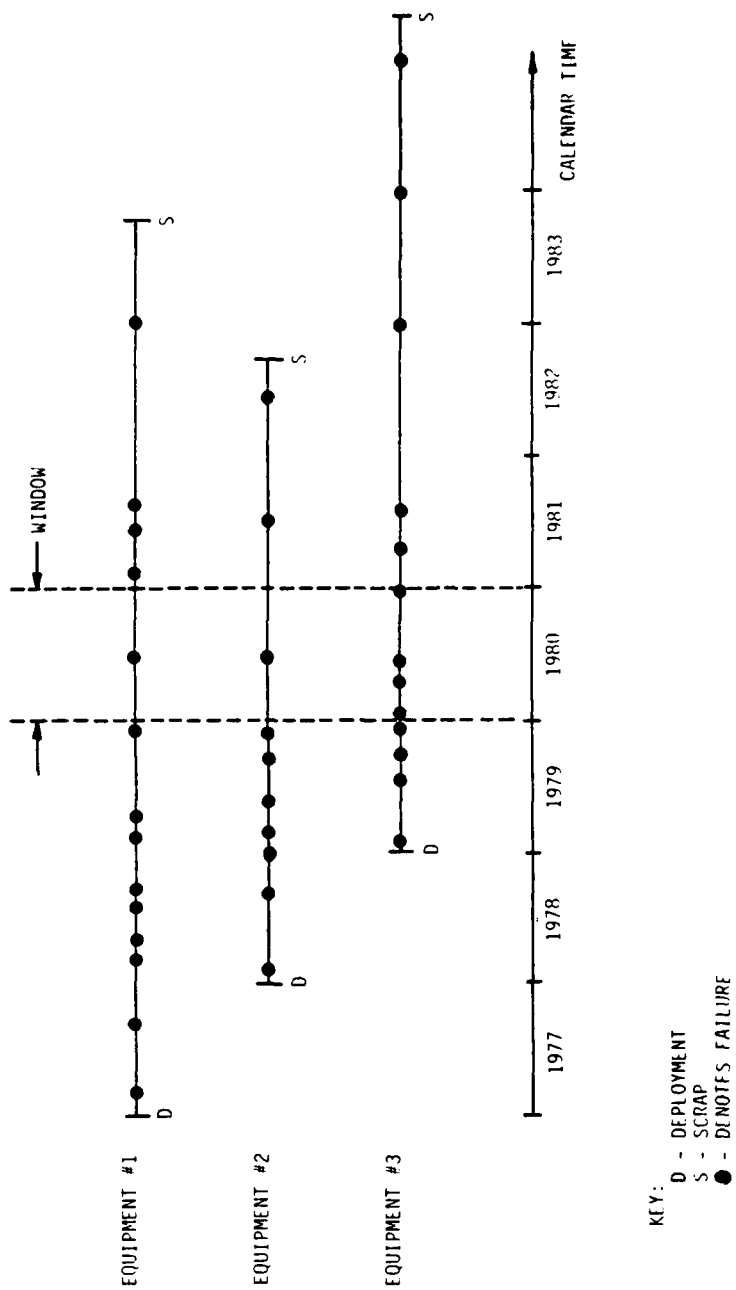
FIGURE 2.2: THE "WINDOW" METHOD OF DATA COLLECTION

showing no time dependance will appear identical to failure data where no information is available regarding time dependencies. It is the responsibility of the analyst to properly interpret the meaning of time zero in his/her data set.

Even in those cases where a reasonable quantity of data is available, the data is of limited utility because of built-in bias and sampling errors in the data. (In the case of hybrid microcircuits, over 90% of all available field data was on hermetically packaged hybrids in avionics equipments. As a result it was virtually impossible to discern the effect of environment and package type (these factors were addressed by other means).

Thus "quality" data must have the attributes of accuracy and completeness, as well as utility and balance. (In a statistical sense, balanced data is equally weighted in all categories of interest.)

In the performance of this contract, the primary data problems were unbalanced data and insufficient data. Further explanation of these problems and the ways these problems were addressed will be discussed later in this report.

2.1.4 Statistical Problems

Some difficulties were encountered with the data collected, and the study requirements which either precluded or restricted the applicability of standard statistical analysis methods. These difficulties are defined as follows.

2.1.4.1 Grouped Data

In order to statistically analyze failure data using standard distribution theory, individual component failure times are required. For most life test data, and for all field data, information on individual

failure times is unavailable; data are instead grouped into certain numbers of failures (r) in certain total part operating (or test) hours. This is illustrated graphically in Figure 2.3.

8 Components used in a given equipment operating over time t_0 to t^* failure times (t_i) known

IDEAL DATA

Same 8 components, same (t_0, t^*) t_i not known

?

PRACTICAL DATA

t^* 4 Components out of 8 failed
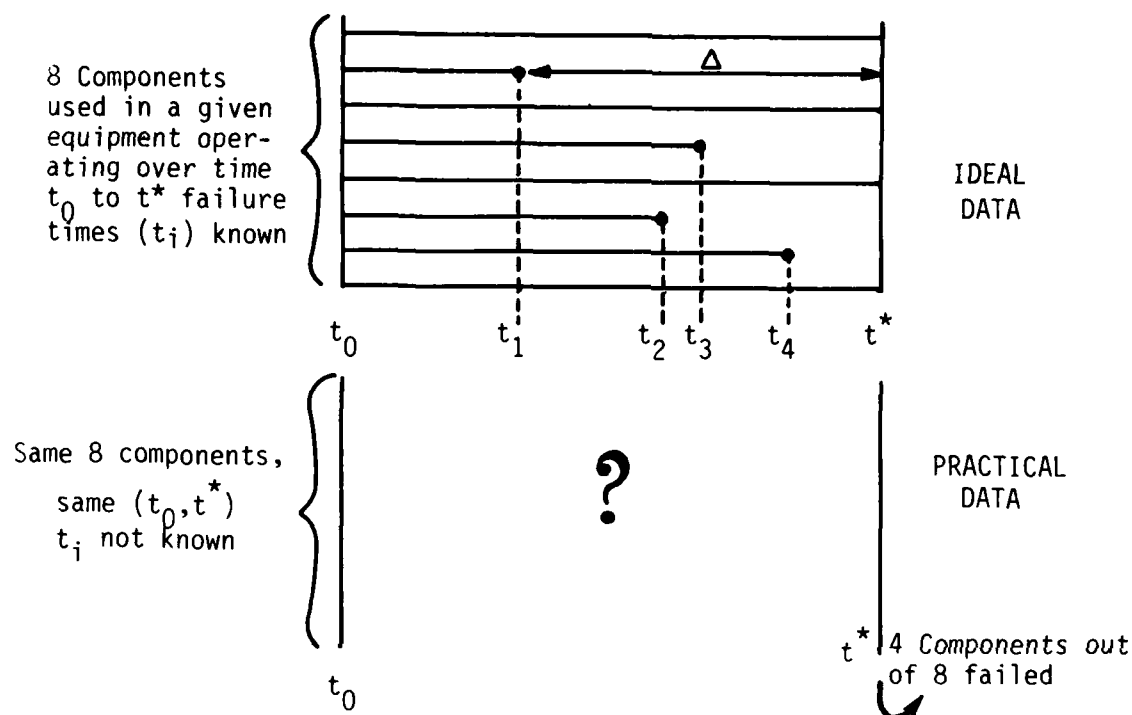
FIGURE 2.3: GROUPED DATA

This type of data problem arises because tests and operating conditions from which reliability data are collected, are not designed for purposes of assessing failure rate. Thus some inspection interval t_0 to t^* is defined by constraints (such as maintenance or sortie length) which are essentially arbitrary as far as reliability assessment is concerned. In addition to the resultant grouping effect on the data, there is also some introduction of noise through not knowing where (in the inspection interval t_0 to t^*) the failure(s) occurred. An example of such noise is shown as Δ in the figure above.

Some work was carried out toward a solution of the statistical aspects
of this problem. In the final analysis, the sparsity of the data tended
to over-ride its grouping effect. The problem is now subdivided into
three categories; homogeneity, regression and noise.

2.1.4.1.1 Homogeneity

For complete data under given conditions with individual failure
times, one can apply outlier tests to individual data points to see
whether they may be assumed to have come from the same distribution. It
is necessary to establish this condition (homogeneity) to validate
subsequent statistical analysis. It is also possible to perform goodness
of fit tests on the data set as a whole, to establish its failure
distribution (as exponential, Weibull, or whatever). For grouped data,
neither technique is applicable. A solution is as follows:

Assuming the underlying failure distribution is exponential, given by

$$f(t) = \lambda e^{-\lambda t} \tag{1}$$

where

$f(t)$ = is the probability density function (p.d.f)
λ = is the failure rate
t = is time (part hours)

Then, since we have r failures grouped, we require the distribution of
the time to r^{th} failure $f_r(t)$ which is given by the gamma density

$$f_r(t) = \frac{e^{-\lambda t} \lambda^r t^{r-1}}{(r - 1)!} \tag{2}$$

Instead of considering the time to r^{th} failure, it will be convenient
to consider the mean time to failure as evaluated from r failures, which
is simply t/r.

Putting $\tau = t/r$, from (2), and applying standard distribution theory,

$$f_r(\tau) = f_r(t) \quad \frac{dt}{d\tau}$$

where

$f_r(\tau)$ is the p.d.f. of τ, the mean time to failure (MTTF) evaluated from r records.

$$\therefore f_r(\tau) = \frac{r\lambda(r\lambda\tau)^{r-1} e^{-r\lambda\tau}}{(r-1)!} \tag{3}$$

Thus if we have a set of data, (as is found in practice) with a variety of r, the distribution of the observed MTTFs is simply a superimposition of the $f_r(\tau)$ for the range of observed values of r. Solution of the compound distribution of $f_r(\tau)$ required Monte Carlo simulation. The solution, and simulation program may be used to check the homogeneity of data sets, and to establish approximate confidence intervals for failure rate.

If conditions vary (e.g. environment, screen class, technology etc.) which is invariably the case for real data, their effects are removable by covariance analysis and regression prior to the homogeneity testing defined here.

2.1.4.1.2 Regression

Standard regression and covariance analysis is used (as discussed in section 2.1.5.2). However, again, these methods require individual rather than grouped data. Our solution here is largely intuitive though mathematical empirical verification is easy.

Regression analysis using the observed failure rates would place equal weighting on a failure rate derived from (say) 100 failures, as it would on a failure rate derived from a single failure. It would seem that the

first observation should be given far more weight. Notice also the effect on variability about a fitted regression line. If λ is the dependent variable then a model of the form

$$\xi(\lambda) = b_0 + \beta_1 X_1 + \beta_2 X_2 + \dots \beta_n X_n + \epsilon$$

will be fitted where ξ is some suitable transform function such as logarithmic required to linearize the regression and normalize the residuals. The X_i are independent variables (such as environment, junction temperature etc.) and the b_i are the regression coefficients. ϵ is the residual variation about the regression. Figure 2.4 below clarifies this discussion.
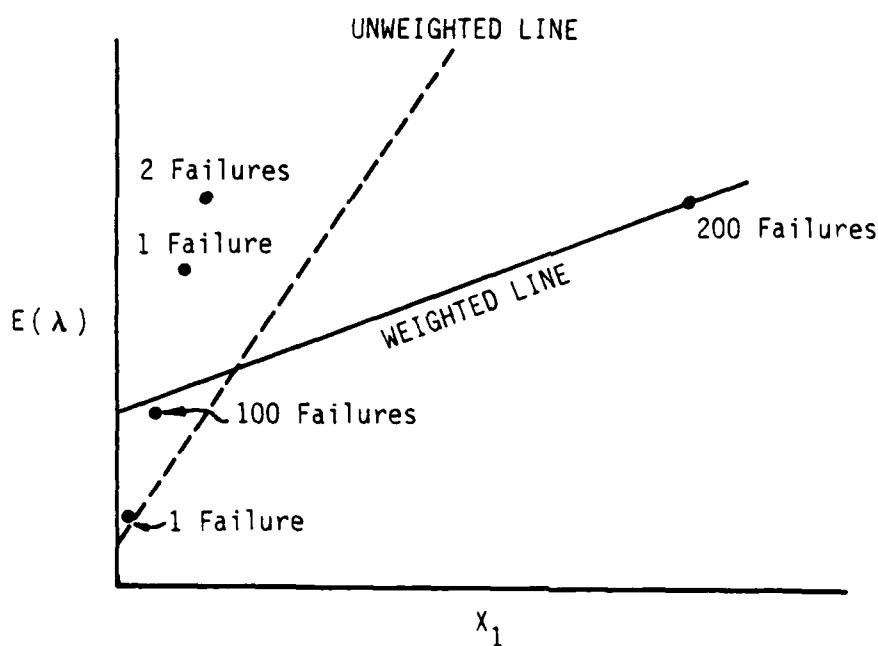
FIGURE 2.4: WEIGHTED REGRESSION

Now, grouped data will have less residual variability, where "less" really means "by factor of r." This happens because, if ϵ is distributed for individual observations as normal with variance σ^2, the variability of

grouped observations will be σ^2/r. Traditionally, regression with unequal variance is treated using inverse variance weighting, i.e., r/σ^2, which reduces to weighting each data point by (r - the number of failures that gave rise to it). This result is readily verified empirically by solving a simple linear regression with individual observations, then grouping some set(s) of the data, weighting by r, re-regressing and finding the same result as was found for the raw data.

2.1.4.1.3 Noise

It is not possible to actually eliminate measurement noise since times of individual failures are not recorded. It may be possible to statistically solve and eliminate the noise, but this was considered unnecessary in view of the sparse data available. Application of some statistical treatment would require large good quality data sets, which are just not available.

It will be noted that the effect of the noise will always be to <u>over</u> estimate the time to failure, i.e. <u>under</u> estimate the failure rate. It is hoped that part MTTF will be so large in comparison to inspection intervals, and number of parts on test so large in comparison to numbers failed, as to reduce the noise to an insignificant level.

2.1.4.2 Zero Failure Data

Failure data on electronic components are inevitably a restricted sample in view of their expected MTTF being of the order of 10^6 part hours. In many cases, this is much longer than the technology has been available and, however good the sample, it can only cover the first few percentiles of the probability density function. Figure 2.5 clarifies this for an exponential TTF distribution.
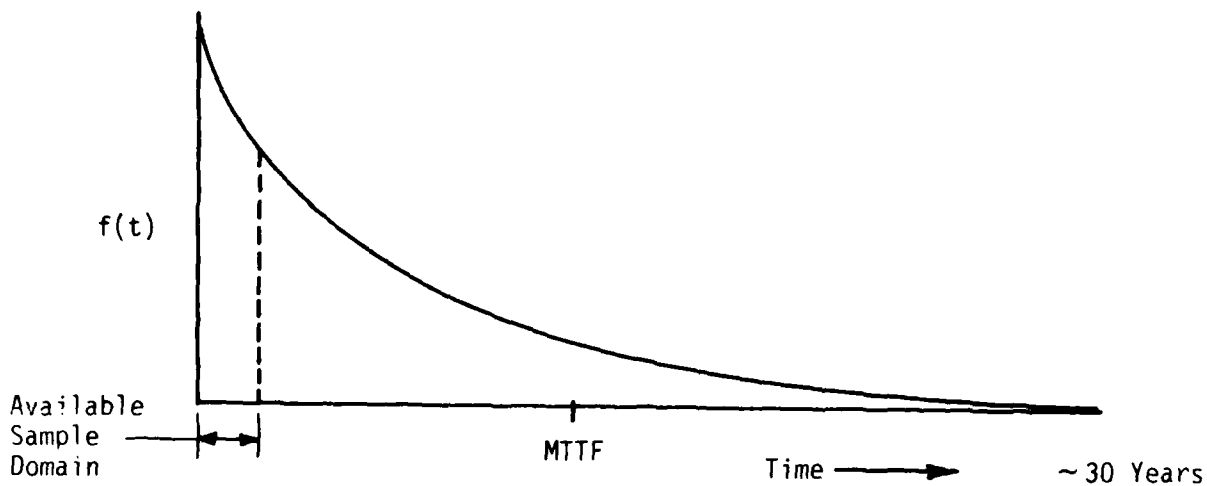
FIGURE 2.5: RESTRICTED SAMPLE DOMAIN, EXPONENTIAL TTF DISTRIBUTION

Now, provided the failure rate is constant (i.e. exponential failure model), this restricted sample domain is not troublesome so long as the operation times are not ridiculously small (although it is true that the greater the operating hours, the greater the precision in the failure rate estimate). However, it is necessary to include the operating times for the survivors (i.e. the parts which did not fail yet). If the surviving parts are not included, the resultant failure rates derived will be for the early failing parts, which will tend to error pessimistically. Now, for estimating failure rate under a given set of controlled test conditions there are standard means of accommodating this type of problem, which is termed censoring. Since field reliability data are not yielded under controlled conditions (rather, conditions vary in a complex, uncontrolled fashion), it is not straightforward to accommodate survival data. Previous work of this type has used an upper confidence limit $\lambda*$ given by

$$\lambda* = \frac{\chi^2_{2,\ 1-\alpha/2}}{2T}$$

2-29

where

χ_2^2 is the chi-square statistic with 2 degrees of freedom

$1-\alpha$ is the confidence level chosen

T is the total test time (part hours)

Though this is a good practical solution, its theoretical basis is unfounded, in particular the analysis or combination of confidence intervals is undefined. Use of this approximate method would also require some minimum T to be defined to avoid unmeaningful failure rate estimates from very low survival times. A simple way of doing this would be to define the minimum T as indicated by the data. An alternative would fit a model of the form $\lambda^* = aT^b$ to the total test time. This would have the beneficial effect of weighting each λ^* in relation to its total test time and would also be applicable to failure rate estimates for which failures did occur (since we would expect some increased precision with T, for failure data also).

An alternative solution would be to combine data observed under identical conditions using standard censoring formula. Though the wide variety of conditions makes this difficult, it could be effected in crude groupings of variables.

Figure 2.6 below illustrates.

COMBINE FOR MLE

$1/\hat{\lambda}$

(Hours)

X_p

● FAILURES

○ ZERO FAILURE
   TRUNCATIONS

MLE = Max. Likelihood
Estimator of $1/\hat{\lambda}$ for
given value of X_p with
all other X_i constant
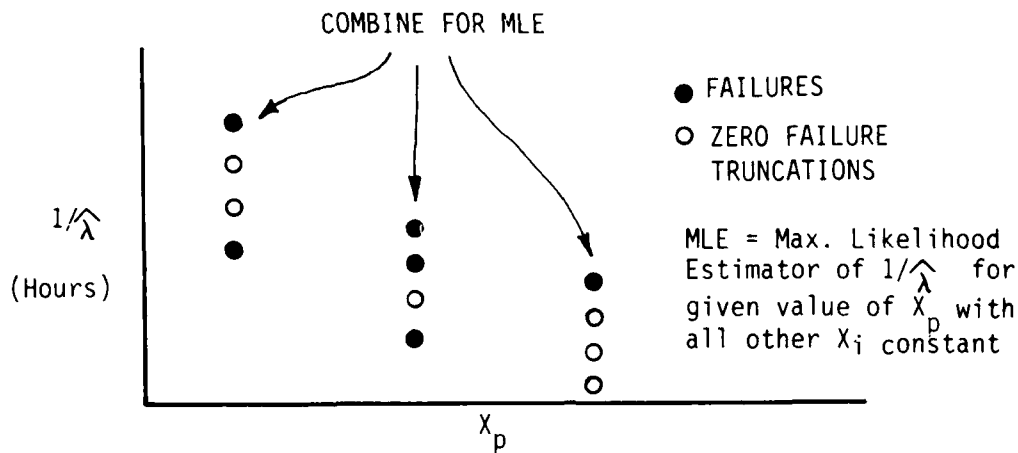
FIGURE 2.6: COMBINED CENSORED DATA

2.1.4.3 Unbalanced and/or Sparse Data

Statistical analysis of multivariate data does assume balanced samples, meaning that the full range of each variable is equivocally represented in the sample. Though theoretical methods do exist for unbalanced samples, they rapidly become complex and do not readily extend to the severe problems of field reliability data. Indeed, in some instances, no data is found, e.g. for Class S hybrids. Since such problems are clearly insoluble, our approach was to at least understand what effect the imbalance and sparsity of the data would have on the analysis. The most powerful way to do this is by use of flexible graphical methods such as scatter plots. These are fully defined in Section 2.1.5.1.

2.1.5 Statistical Methods

In addition to the special considerations of the previous section, standard statistical analysis methods were used. These are divided into

two sections, exploratory and analytical. The exploratory methods are used to formally test hypotheses and to fit the prediction models.

2.1.5.1 Exploratory Methods

The most effective way to initially study a set of data is to plot it. Most library computing routines include a scatter plot program: However, since a method was required which would also plot r (the number of failures per record) and provide some graphical assessment of zero failure data, a new program was written. This provided a valuable, fast means of looking at the data in all stages of analysis.

The program is designed to read a given data file, calculate the MTTF for each record and plot MTTF against the independent variable of the user's choice.

Zero failure data is also accommodated simply by constructing an upper confidence bound on the total test time and setting r=o. The program when implemented, simply plots r against the user specified axes.

2.1.5.2 Statistical Analysis Methods

2.1.5.2.1 Multiple Linear Regression and Covariance Analysis

Multiple regression analysis is used to fit a mathematical relationship between a dependent variable (in this study, failure rate) and given independent variables found to influence the dependent. Such independent variables might include die size and number of bits (for VLSI); substrate area and number of diodes (for hybrid devices).

For linear regression analysis, a model of the following form

$$\lambda = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \ldots + \beta_n X_n + \epsilon \tag{1}$$

where

λ is failure rate (the dependent variable)

β's are coefficients

X_i are the independent variables

ε is the residual variability, i.e., the difference between the observed and the predicted failure rate.

A set of data on λ together with readings of the X_i may be used to solve for the β's using least squares theory. This method essentially minimizes the squared residual errors and makes certain assumptions in doing so, which are listed as:

a) the X_i must be independent of each other (i.e. have zero covariance)

b) the X_i should be measured without error

c) the auto-correlation of the ε for a given data set should be zero

d) the residual variability should be the same for all values of all the X variables (homoscedasticity).

In practice, assumptions a) and d) were often violated by the data employed in this study, though b) and c) were satisfactory. Violation of the assumptions is inevitable to some extent, and we add the precautionary notes that

o   Regression statistics such as F, R^2 and use of standard errors become approximate.

o   Regression conclusions should be verified by exploratory analysis and by critical engineering review.

Subsidiary statistics generated as a part of regression analysis allow the following questions to be answered:

o   How good is the fit?   This is measured by the coefficient of multiple determination (R^2) by assessing its proximity to unity. In percentage terms, $100R^2$ defines the percentage of the overall variability accounted for by the regression model.   Thus R^2 varies between 0 and 100%.

o   Which variables affect failure rate?   If certain assumptions of error normality and auto-correlation hold true, the F statistic may be used to objectively measure the significance of each variable, with respect to its effect on failure rate. Essentially, the statistic works by comparing the fitted model (for each variable separately) to the residual variability.   If the effect of the variable significantly exceeds the residual variability then, statistically, the conclusion is that the variable affects failure rate.   If the effect of the fitted variable is less than the residual variability, then it is concluded that the variable has no effect (or at least if it does, the effect is negligible, and leaving it out of the final model will matter little).   The F statistic is analagous to a signal to noise ratio in electronics.

o   Is there a better fit?   If certain conditions are met by the sample, it is possible to statistically evaluate when to sample and it is possible to statistically evaluate when to stop trying for a better fit.   It is unwise to try for too good a fit by introducing more and more variables.   Conversely, it would be easy to attain an extremely high R^2 value, but this would merely result in modeling the noise, and the fitted model would not be repeated in a separate sample.   In the data for this study the required conditions for establishing whether there is a better fit were not met.   We therefore imposed the generally accepted rule of thumb that no more than six or seven variables be fitted.

The linear model, as defined in (1) above, is unlikely to fit reliability data without certain transformations. For example, the effect of temperature on failure rate is well known to be inversely logarithmic and hence not accommodated by the simple linear model. Mathematically, this example may be written

$$\lambda = \exp \quad -\frac{E_{oa}}{k} \ (1/T) \hspace{4cm} (2)$$

where

λ is the failure rate

E_{ea} is equivalent activation energy

K is Boltzmann's constant 8.63 X 10^5 eV/^oK

T is junction temperature in absolute units (^oKelvin)

The relation between λ and T is therefore, clearly, not linear though it is intrinsically linear. The intrinsic linearity may be converted to linearity by a transformation. Here the transformation is logarithmic. Hence, applying to (2):

$$\log \lambda = -\frac{E_{ea}}{k} \left(\frac{1}{T}\right)$$

and the inverse linear relation is now established. Various transformations on each of the variables can yield a wide variety of models, soluble using linear methods, which are far easier than non-linear models. The type of transformations, and the form of the resultant theoretical models are discussed in detail under section 2.1.6. This section is concluded using the simple model (1) for ease of comprehension.

The regression solution is tedious by hand, and computer solution was used. The commercial program SMLRP (Stepwise Multiple Linear Regression Program) was used. This program prints out, in addition to the regression solution, a correlation matrix for the linear correlation between each pair of variables, as well as means, standard deviations and extremes of each variable. Finally, the fitted model is assessed by a printout of the residuals (i.e. observed -predicted failure rate). The residuals should show a pattern like this (random)
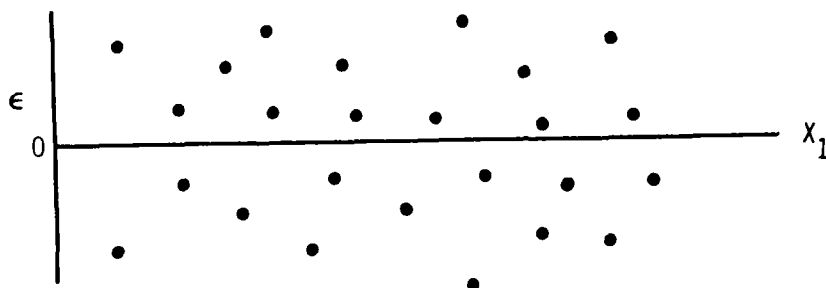
rather than either of these
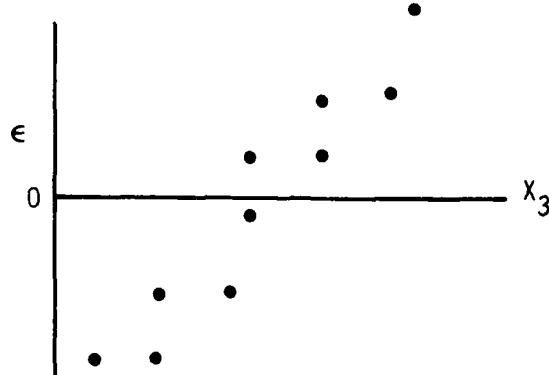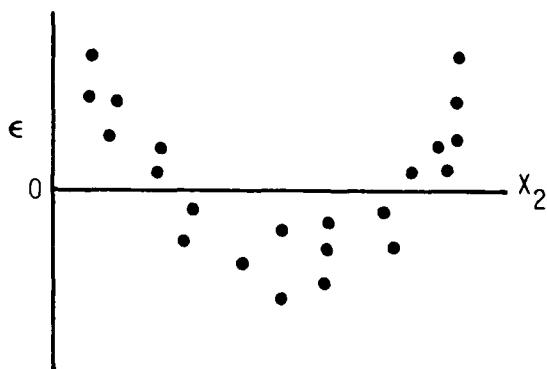
The latter patterns would indicate either that one or more significant variables had not yet been fitted, or that a fitted variable had been incorrectly transformed.

Covariance

The regression procedures defined so far can only be applied to continuous variables such as die size, substrate area or number of bits. However, where variables are discrete (i.e. qualitative) further methods are required. For example, if the effect of technology is to be studied, there is no numerical relation between TTL and CMOS, though it may be found that one exhibits higher failure rate than the other. Covariance analysis may be used to extend least squares solutions to discrete variables. Continuing with the TTL/CMOS example, a dummy variable X_1 could be defined as

$$X_1 = \begin{array}{ll} 0 & \text{TTL} \\ 1 & \text{CMOS} \end{array}$$

Then using model (1), solution for a set of data will give $\lambda = \beta$ for TTL data and $\lambda = \beta_0 + \beta_1$ for CMOS data (where the β_0 and β_1 are the regression solutions).

If there are more than two cases to be covered by a dummy variable then more than one dummy variable will be required. For example, if we also consider ECL devices, then variables X_1 and X_2 are defined such that,

$$X_1 = \begin{array}{ll} 1 & \text{CMOS} \\ 0 & \text{TTL} \end{array}$$

$$X_2 = \begin{array}{ll} 1 & \text{ECL} \\ 0 & \text{TTL} \end{array}$$

thus, solution of the model $\lambda = \beta_0 + \beta_1 X_1 + \beta_2 X_2$ gives $\lambda = \beta_0$ for TTL, $\lambda = \beta_0 + \beta_1$ for CMOS, and $\lambda = \beta_0 + \beta_2$ for ECL.

If there are transformations involved, the dummy variable applies <u>after</u> transformation.

For example if the model is of the form

$$\lambda = \beta_0 X_1^{\beta_1} \tag{3}$$

then logarithmic transformation gives

$$\log_e \lambda = \log_e \beta_0 + \beta_1 \log_e X_1 \tag{4}$$

and the covariate is now

$$\log X_1 = \begin{array}{ll} 0 & \text{TTL} \\ 1 & \text{CMOS} \end{array}$$

The method is readily extended to more than one discrete variable (e.g. environment, screen class, etc.).

The regression statistics and selection of significant covariates applies as for continuous variables.

2.1.6 The Theory of Models

There are three forms of statistical models, which may be fitted by regression analysis, whose purpose are respectively

o   to study
o   to predict
o   to control

The models to be fitted in this study are required to fulfil all three of the above.

Study Models

These models are set up to study the effect of any given variables on failure rate.   One of the purposes of this study is to assess which factors affect failure rate.

Prediction Models

These models are designed to provide a relation between λ and the independent variables which may be used to estimate failure rate, given the values of the other variables.   Though the models of MIL-HDBK-217 have been commonly referred to as prediction models, their implementation is really only a practical estimation procedure and is not predictive in the statistical sense (e.g. of time series).   A good prediction model will use suitable variables indicative of reliability.

Though this is largely semantics, users have encountered difficulty attaching error bounds to the point estimates, as would normally be the case with a prediction model.   It was therefore resolved to include error

2-38

bounds on individual predictions or confidence intervals on the fitted parameters, or both.

Control Models

Control models also establish mathematical relations between two or more variables, but use one or more of the variables to control some dependent variable. In this study, it is a requirement that the failure rate be controlled by assigning appropriate regression parameters to variables known to degrade reliability. A good control variable will influence reliability but need not necessarily be a suitable predictor variable (e.g. a quality plan).

VLSI, Hybrid and Analog Microprocessor Models for MIL-HDBK-217

The required models for VLSI, hybrid and analog microprocessor data are required to study, predict and control. Though this can be achieved to a reasonable approximation, the performance in any one category may suffer as a result, since good indicator variables for prediction models may not coincide with good control variables.

Fortunately, many reliability factors serve well both as predictors and controller (e.g. temperature).

Model Structures

The precise forms of models considered for this study are now defined.

The Additive Model

As already defined in (1), the additive model relates the failure rate to a linear combination of independent variables. This model is unlikely to apply to reliability data, except perhaps partially (for a single variable added to some other model structure).

2-39

The Multiplicative Model

There is considerable empirical justification for using a multiplicative model of the form

$$\lambda = \beta_1 X_1 \times \beta_2 X_2 \times \ldots \beta_n X_n \times \epsilon \tag{5}$$

This essentially says that each increase in any X_i increases the failure rate, λ, by a certain proportion. Since a logarithmic transformation is required to convert (5) to a linear model, zero values of any X_i causes problems since $\log 0 = -\infty$. However, a practical solution is generally achieved by substituting some small positive value for the 0.

The Exponent Model

A popular regression model due to Cox is the proportional hazards model given by

$$\lambda_p = h(t) \; e^{\beta_0 + \beta_1 X_1 + \beta_2 X_2 + \ldots \beta_n X_n + \epsilon} \tag{6}$$

where

λ_p is the predicted failure rate

$h(t)$ is the hazard rate

This model (equation 6) has the attractive property that it can be reduced to a multiplicative one without problems of logarithms of zero, viz:

$$\lambda_p = h(t) \; e^{\beta_0} e^{\beta_1 X_1} e^{\beta_2 X_2} \ldots e^{\beta_n X_n} e^{\epsilon} \tag{7}$$

Then, assuming a constant hazard rate gives

$$\lambda_p = \alpha e^{\beta_0} e^{\beta_1 X_1} \ldots e^{\beta_n X_n} e^{\epsilon} \tag{8}$$

The Polynomial Model

Models of the form

$$\lambda = \beta_0 X_1 + \beta_1 X_1{}^2 + \beta_2 X_1{}^3 \text{ can be useful.} \tag{9}$$

Isolated terms of the form

$$\lambda = a X_i{}^b \text{ may also be useful.}$$

They have the characteristic (which previous transformations do not) of λ being zero at $X_i = 0$. (whereas $e^{X_i} = 1$ at $X_i = 0$).

The VLSI, Hybrid and Analog Microprocessor Models

Inevitably, the fitted models include combinations of the previous four models. The general model fitted was of the form

$$\lambda_p = \alpha e^{\beta_1 X_1 + \beta_2 X_2 + \beta_3 X_3 + \cdots} e^{\frac{Eea}{K} \left[\frac{1}{T + 273} - \frac{1}{298} \right]} \alpha t^\gamma \epsilon \cdots \tag{10}$$

Where the symbols are as defined before, and α and γ are constants. The αt^γ term was included to remove the effect of differing test times and (particularly) very small survival times. The X_i include both continuous and discrete variables.

3.0 VERY LARGE SCALE INTEGRATED CIRCUITS (VLSI)

Continued advancement of the state-of-the-art in integrated circuit fabrication and processing techniques has created an electronics industry which is in a constant state of flux. As a result, the microelectronic reliability prediction models of MIL-HDBK-217 require frequent revision to keep them current with the state-of-the-art. Such is presently the case. LSI technologies are becoming routine; the industry is rapidly advancing to very large scale integration (VLSI) and beyond. Densities of 50,000 devices on a chip are now achievable, with 1,000,000 devices on a chip predicted for 1986. A second generation of microprocessors and peripherals is now available, with sophistication and capabilities that simplify their use, as well as making feasible designs which were previously impractical.

These new devices, with their ultra-small geometries, extremely high densities, large die sizes and even larger package sizes have introduced a number of unique reliability problems as well as emphasizing the need for solutions to old problems.

Present VLSI devices are taxing the constraints of existing fabrication processes and equipments. Geometries are approaching (and often exceeding) the limits of conventional photolithographic techniques. (When dimensions of features approach the wavelength of light, resolution falls off rapidly.) As a result, new techniques such as electron beam (E-beam), ultraviolet, and x-ray lithography are becoming common. Also a problem is the chemical etching process used to define the metallization pattern on the chip, where line widths and spacings are being limited by the manufacturer's ability to control the process. New diffusion techniques have been adopted due to limitations in the conventional photolithographic mask generation and registration processes.

The price paid for using new and innovative state-of-the-art fabrication techniques is that of an immature process with its associated

3-1

potential reliability problems. Unfortunately, most VLSI components presently being manufactured cannot be handled by the existing reliability prediction models of MIL-HDBK-217C.

Second generation microprocessors present a particular problem when trying to estimate their reliability with the existing MIL-HDBK-217 models. Most second generation microprocessors (or microcomputers) have on-chip memory (RAM, ROM, EPROM, etc.). Existing techniques provide separate models for random logic devices and each of the memory types yet have no provisions for chips which include both random logic and memory functions. Many such devices are now available, with many more in the planning stages; a partial list is contained in Table 3.1.

In addition, a number of 16 bit microprocessors (such as the Texas Instruments 9900, the Motorola 68000, and the Intel 8086) are now or will soon be available. Several 32 bit microprocessors are in the final development stages. These devices are vastly more complex than their 8 bit predecessors. Gate counts have increased by an order of magnitude or more. Furthermore, the interface and support circuits needed to utilize these complex CPUs are also becoming very complex. Programmable Input-Output (PIO) chips, Universal Asynchronous Receiver Transmitters (UART), Peripheral Interface Adaptors (PIA), analog to digital (A/D) and digital to analog (D/A) converters, and a host of other support chips have been scaled and redesigned to accommodate the 16 and 32 bit processing units. In some cases these new support chips are more complex than were early microprocessors.

In the VLSI memory area, single chip monolithic memories are now available with 64K (65,536) bits. Memories with 128K and 256K bits are in the planning states. The 64K RAM is being produced with limited success using conventional microcircuit fabrication procedures. These devices are severely taxing the capabilities of existing manufacturing techniques, however.

3-2

TABLE 3.1: SUMMARY OF MICROPROCESSORS CONTAINING ON-CHIP MEMORY

Manufacturer	Part Number
AMI	68A02/08
	52200
	52300
	52150/A
Fairchild	F3876
	F3878
	F3870 Series
Intel	8021
	8022
	8051
MMI	6701
Mostek	MK 3870 Series
	MK 3850
Motorola	6805 PZ/R2
	146805 EZ/62
OKI	MSM5840
Rockwell	PPS-4
	PPS-4/2
Texas Instruments	TMS-9940
	TMS-1000
Zilog	Z8

Aside from the production problems, the extremely small geometries of these high density memories have resulted in some new failure mechanisms which do not affect larger geometry circuits. For example, with very small geometries, the total charge in any given memory cell is so small as to be susceptible to a variety of environmental effects which are harmless to smaller scale integrated circuits. Recent literature has given particular attention to the problem of background alpha particle radiation and its effects on VLSI memories. It has been found that even low energy alpha particle radiation originating from ceramic microcircuit packaging materials is capable of causing bit errors in memories. The alpha particle penetrates the chip, ionizing sufficient atoms in the chip to produce a net charge comparable to that in an individual memory cell, resulting in an erroneous logic state.

IC manufacturers are addressing this problem in a number of ways, including the use of low background radiation materials, the addition of die overprotection to prevent alpha particles from reaching the die, and designs which result in a greater total charge per memory cell.

The problem of soft errors in memories, and the problems with low yields due to random defects have resulted in a variety of new design and processing techniques intended to address these particular problems. A number of error detection and correction chips have been developed; both of the stand-alone (discrete IC) type and, in some instances, built into the memory chip itself, although to our knowledge, none of the latter type are commercially available at the present time. The net reliability impact of such circuitry must be carefully studied.

Another new technique is the use of redundant bit lines in VLSI memories to improve the fabrication of extra memory locations on the chip. When wafer fabrication is completed, the individual chips on the wafer are probed and tested to identify any faulty locations. Any such locations are then separated from the remainder of the circuit by means of fusible

links or selective wire bonding to the package pins. In this way, less than perfect chips can be used as 100% functional memory devices.

Such a technique can only be successful if it can be shown that the failure mechanism causing the fault in the first place will not degrade the performance of other portions of the chip at any time. Considerable work has been done in an attempt to prove that this is indeed the case. (for further reference, see the Proceedings of the 1981 International Reliability Physics Symposium, pp 1-10, "Redundancy Reliability" by Crook and Meyer. This paper suggest that, with due care in manufacturing and proper component screening, that LSI microcircuits using redundant sections to improve yield are as reliable as any in the industry).

In future devices, manufacturers will be adding one or more bits to each word in the memory. These extra bits will be used as parity bits for on-chip error detection and correction schemes. The effectiveness of such schemes for reducing incidence of soft errors will probably be a function of the sophistication of the technique as well as the type of error-inducing mechanism present. In the case of ionizing radiation, the chip layout may be an important factor. For example, if all bits in a word are in close physical proximity on a chip, the localized ionization currents could induce multiple bit errors in a given word, whereas if the word bits are distributed over the chip, the probability of multiple errors in a single word should be reduced.

In a future generation device using redundant memory locations, the selection algorithm may be built into the chip, with testing and selection of functional locations being done automatically by internal logic. This technique would allow the instantaneous selection of a new (functional) bit line should a previously selected line fail during operation.

While the above mentioned techniques represent desirable and useful techniques for improving the reliability of future VLSI memories, they do not represent the simple evolution of previous technology. The

3-5

reliability impact of such techniques must be carefully studied. Complexity definitions must be scrutinized. Indeed, the basic definition of a failure may require modification in the case of soft errors.

These and other problems encountered in the evaluation and analysis of the reliability of VLSI devices will be addressed in the following sections.

3.1 VLSI Model Development

3.1.1 Complexity

Prior to a full scaled statistical analysis and modeling effort, a number of specific problems had to be addressed. Foremost among these problems was the issue of an appropriate complexity factor for VLSI devices.

In the past, MIL-HDBK-217 failure rate prediction models for microcircuits have used the number of gates, bits or transistors on the IC chip as a measure of complexity. This complexity measure was then used as an input to the prediction model and, in general, the more complex the device, the higher the failure rate.

There are problems with using this method for VLSI devices, however. First, VLSI devices are no longer "building blocks," but more like "systems on a chip." As such, there are digital, memory and linear functions all on the same chip so that complexity must now be addressed as a linear combination of the number of gates, bits and transistors:

Complexity = α_1 (No. of gates) + α_2 (No. of bits) + α_3 (No. of transistors)

This by itself might be manageable. However, the extreme integration employed in the fabrication of VLSI devices makes it virtually impossible

3-6

to count the number of gates, etc. on an IC chip. Furthermore, as computer-aided design becomes more popular, even the manufacturer has no way of determining the number of discrete components on the IC chip.

Standard memory devices are somewhat easier to contend with than are random logic circuits, since they are usually manufactured in specific sizes, for example 64K bits or 16K bits. As a result, complexity is accounted for by the size of the memory chip. In our preliminary analysis it was found that the observed failure rates for VLSI memories found in our database did not differ significantly from the failure rates predicted by the existing semiconductor memory models. As a result of this observation and in light of the limited data on semiconductor memories, it was decided to let the existing models stand unchanged.

In the case of VLSI logic, however, it was found that the present MIL-HDBK-217 models were not doing a satisfactory job of estimating field reliability performance. In many cases, the existing models could not even be used, since there is no obvious way to accommodate logic devices with on-chip memory. This study will not therefore address memory devices, but will limit itself to the evaluation and modeling of VLSI logic devices, with or without on-chip memory.

Given these problems, we found ourselves facing the following questions:

(1) Does complexity impact device reliability?

(2) Even if device complexity does have an effect, is the effect large enough to be significant over the relatively limited range of devices labeled "VLSI"?

(3) If complexity is significant, are there other ways of expressing it than the conventional number of transistors, bits or gates? If so, what are they?

Since complexity is a theoretical concept having no physical meaning, there is no way to correlate failure rate to complexity unless a specific

measure of complexity can be defined. As such, it was necessary to assume that complexity has an impact on reliability, define one or more "reasonable" measures of complexity, and check for a correlation to failure rate. In other words, Question (3) must be addressed before Questions (1) and (2) can be answered.

The following were suggested as possible useful measures of complexity:

o   number of package pins

o   number of package I/O functions (equal to number of package pins whenever no pins are multiplexed)

o   die area

o   a linear combination of bits, gates and transistors which might be arrived at by partitioning the chip into discrete, manageable subsections.

Several of these choices were rejected almost immediately; number of package pins showed no correlation to the presently used complexity measures (e.g. number of gates), nor did the number of package I/O functions. (Pin multiplexing was not as extensively used as was initially conjectured.)

Die area was proposed for use as a viable complexity measure. This required that die area be well correlated to failure rate. This hypothesis, while intuitively appealing, could not be supported by the available data. It was concluded that although area does relate to failure rate, there are other confounding parameters which mask these effects, thereby making die area useless as an indicator of reliability. Regressions of failure rate versus die area showed a correlation of only 6%.

Since area did not correlate directly to failure rate, it was attempted to correlate die area to the number of gates, bits and

transistors on the circuit. This would provide a useful means, for estimating the number of bits and/or gates on a particular chip. A linear model of the form

$$\text{Area} = \alpha_1(\#\text{gates}) + \alpha_2(\#\text{bits}) + \alpha_3(\#\text{transistors}) + \alpha_4$$

was proposed. In fact, the # transistor variable was dropped because of severe data problems.

Results are given comparatively in Table 3.2 below, for a stepwise regression model, regressing area on bits and gates.

TABLE 3.2: CORRELATION OF DIE AREA WITH NUMBER OF GATES AND NUMBER OF BITS

Correlation	Correlation Coefficient (Confidence level 90%)
Area vs. bits correlation (simple linear)	0.323
Area vs. gates correlation (simple linear)	0.899
Bits vs. gates correlation (simple linear)	0.457
R^2 Multiple correlation on Area	86%
Significant variables with respect to area	# gates
Maximum absolute deviation (sq. mils) from fitted model	18565

It should also be recalled that other variables were fitted as well as bits and gates (to remove their effects) but are not reported since they are not of interest. Other variables fitted were number of pins, technology type, and device type. The final relation was solved for a confidence of 90% to yield the following regression equation (with standard errors underneath in parentheses). Bits were not shown as significant for our particular data set.

3-9

$$\text{Area (square mils)} = 10163.1 + 4.096 \text{ (\# gates)} + \begin{cases} 9376.1 & \text{MOS} \\ 0 & \text{otherwise} \end{cases}$$

$$(0.587) \qquad\qquad (4250.8)$$

There appeared to be no significant difference between digital, and other device types such as memories, etc.

At this stage, the tentative conclusion is that area is correlated with gates and bits, though the fitted model can only be defined sensibly for the relation between area and gates. Reducing the regression confidence to force the number of bits into the model resulted in a negative coefficient which is physically unjustified.

In addition to the perceived benefits of area as a complexity measure, there are several potential problems:

o   Many vendors consider chip area to be proprietary; probably not so much because chip area is proprietary as because they fear that chip area will be specified in a control document if widely known. Since chip area is closely tied to yield and thus profits, no manufacturer will submit to control of their chip dimensions.

o   In view of the above, it is common for a specific chip to be scaled down several times during its life cycle. This is done to increase the number of chips per wafer and thus improve throughput. As a result, there may not be any single unique area for a specific chip.

o   The percentage of chip area which is "wasted", that is not used for semiconductor devices, varies widely from chip to chip. As a result, the correlation between chip area and number of devices implemented on the chip is not as good as might be expected. This "wasted" space is used for bus lines, dielectric isolation, and other purposes too detailed to be included on a specification sheet, much less in a reliability model. (It should be noted that silicon real estate is too expensive to be truly "wasted". There are, however, other uses for this real estate beside transistors, gates and bits).

o   Even logic cell size varies considerably as a function of technology and scale. Various technologies require differing logic cell structures and differing fabrication processes for each cell. Further, a specific device may be made in several different

scales, by different manufacturers, or by the same vendor over a period of time.

It is therefore suggested that further work be sponsored by RADC to study the feasibility of die area as a complexity measure.

Considerable time and effort was expended in trying to devise a complexity measure based on a linear combination of the number of bits and gates on the chip. This effort proved difficult for the following reasons:

o   Manufacturers do not provide sufficiently detailed information on their VLSI devices to enable an accurate count using this technique.

o   Block diagrams often represent an over simplified version of how a chip has actually been implemented in silicon.

o   For VLSI devices, this technique is tremendously tedious and time consuming, with little assurance of an accurate count when completed.

Since no complexity factor could be found, and since there was no significant correlation between failure rate and the number of gates or bits on a chip, it was thus decided that complexity is not a significant driver of reliability. (Or, alternatively, complexity is not a good indicator of reliability.)

The model form chosen for VLSI random logic devices (with or without on-chip memory) is

$$\lambda_p = \pi_Q \ (C_1 \ \pi_T + C_3 \ \pi_E) \ \pi_L$$

where

π_Q = quality factor

π_T = temperature factor

π_E = environmental factor

π_L = learning factor

C_1 = chip complexity factor

C_3 = package complexity factor

Other factors were defined as in the following paragraphs.

3.1.2 Temperature Factor

The temperature of an operating device is crucial to its reliability. An estimate of the case temperature T_C is given by

$$T_C = T_A + \theta_{ca} P$$

(10)

where

T_A is ambient temperature

θ_{ca} is the case to ambient thermal resistance

P is the power dissipated at the junction

Equation (10) was applied to the full set of life test data available for VLSI devices.

The data are expected to follow an Arrhenius relationship given by

$$\lambda \propto \exp \quad - \quad \frac{E_{ea}}{k} \quad (\frac{1}{T_C} - \frac{1}{T_r})$$

where

E_{ea} is equivalent activation energy

k is Boltzmann's constant (8.63 X 10^{-5} ev/^{O}K)

T_C is case temperature

T_r is a reference temperature

Thus, a plot of log λ against $1/T_C$ would be expected to be linear and negatively correlated.

3-12

Temperature was found significant at the 10% level ($F \simeq 4.06$) and the fitted model accounted for just over 78% of the overall variability ($R^2 = 0.7809$). A number of other variables were fitted as well as temperature. Solution of the regression model then gave the coefficient of (1/T) as -4386.85

Thus $- \dfrac{E_{ea}}{k} = -4386.85$

Now since Boltzmann's constant = 8.63×10^{-5} then $E_{ea} = 4386.85 \times 8.63 \times 10^{-5}$

$$E_{ea} \simeq 0.379eV \simeq 0.38eV$$

The standard error on the coefficient was given as 2199.8, so a crude 95% confidence interval an E_{ea} is given as 0.189 to 0.568. This relates favorably to the values for VLSI activation energies presently used in MIL-HDBK-217.

The term "equivalent activation energy" is used since activation energies really only apply for individual failure mechanisms and consequently the use of a single activation energy covering all failure mechanisms is an approximation, "equivalent" to the overall effect of all the mechanisms.

Since the range of equivalent activation energies presently used in MIL-HDBK-217 correspond approximately to the 95% confidence interval defined by this study, and since it is well established that different technologies are susceptible to temperature to different degrees, the above results were interpreted as a validation of the existing π_T factors employed in the microcircuit models of MIL-HDBK-217. As such the proposed VLSI model will employ the existing π_T factors in their present form.

3-13

3.1.3 Effects of Environment and Quality Level on Reliability

Due to severe data constraints it was impossible to derive environmental factors and quality factors for the VLSI reliability prediction model from first principles. Working backwards, however, it was shown that, given the limited data available, there was no grounds for rejecting the application and quality factors employed in the existing microcircuit models. Consequently, these factors were adopted without further discussion.

3.1.4 Package Complexity Factor

The extremely limited amount of data available for VLSI components (as compared to SSI/MSI/LSI devices) precluded a thorough analysis of the package complexity factor C_3. Since the available data did not contradict the existing C_3 factor, it was left in its present form. Leadless chip carrier (LCC) packages are considered identical to side-brazed ceramic DIP packages for reliability purposes.

3.1.5 Screen Class (Quality Factor π_Q)

Since all data collected on VLSI devices for this study were of screen class D or D-1, no determination could be made as to appropriate values for military quality parts. A regression on plastic vs. hermetic parts for a confidence level of 0.5, indicated that plastic parts exhibit a higher failure rate than hermetically packaged devices.

This was interpreted as being consistent with the presently employed 2:1 quality factor ratio of plastic versus hermetic parts. As such, the values for the quality factor π_Q were adopted for use in the VLSI model.

3.1.6 Complexity Factor

Since all model parameters have now been fitted except C_1, and since no appropriate formula for C_1 could be defined, it was decided to make C_1 a constant. The proper value of C_1 was defined by setting the observed failure rate equal to the predicted failure rate and solving for C_1. That is

$$C_1 = \frac{\frac{\lambda_0}{\pi_Q} - C_3 \pi_e}{\pi_T}$$

Values of C_1 were thus derived for all available data points. The distribution of all such values of C_1 proved to be lognormally distributed with mean 0.0615. The interval defined by $\bar{C}_1 - s$ to $\bar{C}_1 + s$ was found to be (0.0286 - 0.132).

The proposed random logic model for VLSI devices 100 gates or above is then

$$\lambda_p = \pi_Q \ (0.0615 \ \pi_T + C_3 \ \pi_E) \ \pi_L$$

The lognormal distribution of values of C_1 is indicative of a multiplicative model. Residual analysis showed no dependence on complexity, further verifying that a complexity factor was not needed. Also, the residuals were lognormally distributed with geometric mean equal to 0.93, which would seem to indicate that all important model parameters have been fitted. Figure 3-1 shows the distribution of the logarithm of the residuals for the proposed model.

3.1.7 Analysis of VLSI Bipolar vs. Mos.

A special study was conducted to further analyze the VLSI model to determine its validity for bipolar VLSI components. This was done since the large majority of component failure rates available for this study were MOS.
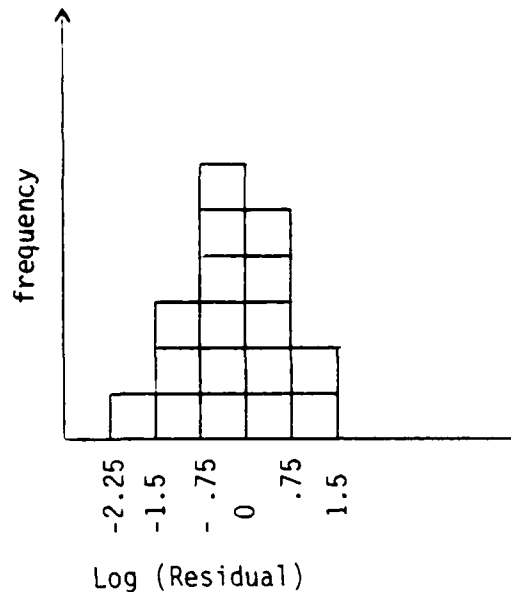
FIGURE 3.1: HISTOGRAM OF LOGARITHM OF RESIDUALS
FOR PROPOSED MODEL FOR VLSI LOGIC DEVICES

Initial re-analysis of the VLSI data indicated a multiplicative factor of 2.19 between bipolar and MOS failure rates. However, on closer inspection, this factor was found spurious since the model fitted presented a poor fit for the bipolar data. Indeed, the bipolar data was in such small quantity and poor quality for the VLSI range of complexities, that no valid statistical model could be fitted. Bipolar technology has not found widespread use in the VLSI range.

In conclusion, although a statistically significant correlation between VLSI Bipolar and MOS devices would not be distinguished, the data available for the bipolar circuits did not contradict this proposed VLSI model.

3.2 VLSI Model Validation

The final proposed VLSI microcircuit failure rate prediction model as presented in Appendix A was used to predict the failure rates of randomly

3-16

selected devices from our database. These predictions were then compared to the actual observed failure rates as a means of validating the model and also as a means of quantifying the error to be expected by users of this model. The results of the analysis are shown in Table 3.3.

TABLE 3.3: VLSI MODEL VALIDATION DATA

Part Number	π_Q	π_T	C_3	π_E	π_L	λ_p	λ_o	λ_p/λ_o
Z80	35.0	.17	.019	0.38	1	0.62	1.27	0.49
6802	35.0	.71	.019	0.38	1	1.78	1.74	1.02
6802	17.5	.38	.015	0.38	1	0.51	0.852	0.60
3870	35.0	.71	.019	0.38	1	1.78	1.39	1.28
8251	17.5	.38	.015	0.38	1	0.51	0.35	1.45
6802	17.5	.38	.015	0.38	1	0.51	0.994	0.51
9080A	17.5	.38	.015	0.38	1	0.51	0.398	1.28
6801	35.0	.71	.019	0.38	1	1.78	0.677	2.63

From this data it would appear that the model will predict the failure rate of VLSI devices within about 25% of the actual observed failure rate. Indeed, the geometric mean of the predicted-to-observed failure rate ratio is 0.995.

Figure 3-2 below has been prepared to give the reader some feel for the behavior of the proposed model under several "typical" circumstances.

3-17
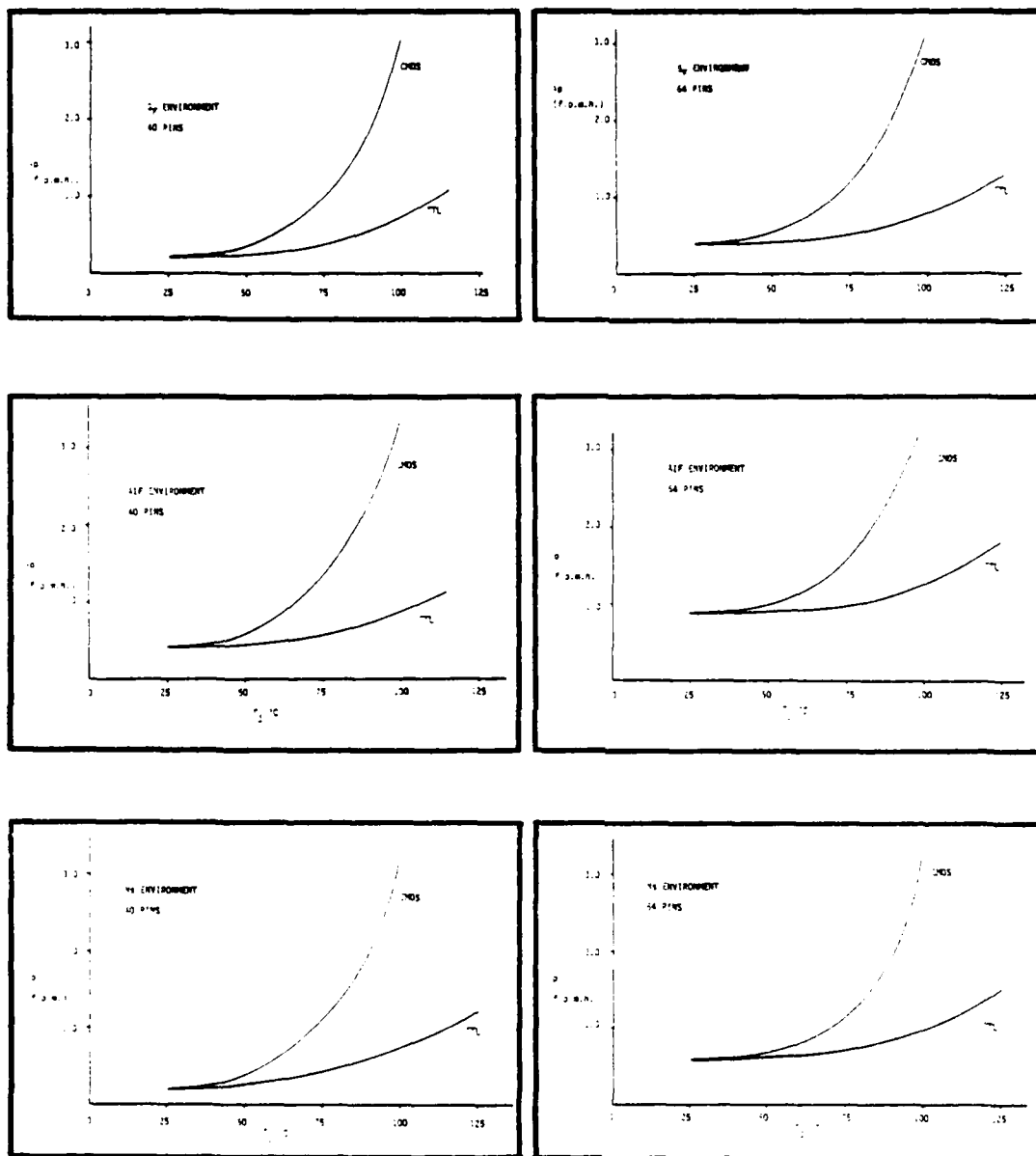
FIGURE 3-2: GRAPHS OF PREDICTED FAILURE RATE VS. JUNCTION TEMPERATURE
FOR THE PROPOSED VLSI MODEL

3-18

4.0 HYBRID CIRCUITS

A hybrid circuit is a microelectronic assembly having characteristics of both an integrated circuit and a printed circuit board. It is analogous to the board-level assembly in that the hybrid is a functional assembly or a building block consisting of a variety of solid state and passive devices connected on a substrate (analogous to the printed circuit board), with electrical paths defined by conductor patterns on the substrate. The hybrid is similar to a small integrated circuit in that the hybrid assembly is contained in a single package which is similar in size, appearance and function to the conventional IC components. Furthermore, the semiconductors within the package are usually in chip form (i.e., no separate package) as in the case of conventional semiconductor components. However, these chips cannot be fully tested over the MIL temperature range.

In the most general sense, hybrids are not as much a device type as a *packaging technology with provisions for multiple devices of various types* and the required conductor patterns to connect these devices in some functional manner. The hybrid device is usually specified, procured, and used in a manner similar to that of the integrated circuit. It is a functional building block which is not considered repairable by the user.

Hybrids can be used in a number of specialized applications where off-the-shelf integrated circuits which meet the design requirements are not available, and the cost of a custom integrated circuit is prohibitive. Hybrid production facilities require only small capital investments as compared to a custom IC facility, making hybrids very cost-effective for small production runs. Since military equipment purchases usually involve relatively small numbers of units, hybrid circuits are an alternative for military applications.

Hybrid technology also offers the designer a means of implementing specialized functions involving very tight tolerances, thermal

4-1

constraints, or other critical parameters which may not be available in conventional ICs. For example, hybrid fabrication techniques allow a high degree of thermal coupling between adjacent semiconductor chips not easily achieved in conventional Printed Circuit (PC) boards. This feature makes thermal compensation circuitry relatively easy to implement in hybrids.

The use of thick film resistors and capacitors allows for the dynamic trimming of these circuit elements in order to optimize one or more critical circuit parameters such as leakage currents, offset voltage, output voltage of a regulator, frequency response of a filter, etc. Trimming is accomplished by removing portions of the thick film element with a laser, abrasive, or other tool. This technique allows for designing precision circuits without the need for matched transistors, precision resistors and capacitors, etc.

The thermal characteristics and small geometries of hybrid components make them desirable in a number of high power/high frequency applications where it is necessary to minimize thermal stresses, thermal coupling effects, parasitic capacitances, spurious emissions, and leakage currents. Hybrid microwave components have been particularly effective on phased array radars, including Cobra Dane, Pave Paws, Cobra Judy and AN/TPS-59.

In spite of the large number of hybrid circuits employed in phased array radars, these equipments make poor data sources. Most of the interesting microwave devices are used in the array assembly. Unfortunately, the array assembly is computer controlled (steered) in order to direct the beam according to the operators wishes. As a consequence, modules near the center of the array see a duty cycle approaching 100%, whereas modules near the periphery may see a duty cycle of 10% or less. As the failure information never gives details as to the location of the failed module in the array, operating times for failed modules are at best only crude estimates. Further any estimated operating

time would result in estimated failure rates so noisy as to mask any other parameters which may influence reliability.

Further hampering the collection of useful reliability data on microwave hybrids is their propensity to incinerate upon failure. It is not at all unusual to open a failed microwave device only to find a molten mass of metal and silicon. Causes of failure are difficult to identify. Judgements as to primary versus secondary failures are also difficult to identify.

Hybrid technology is also important in those applications where minimum weight and maximum component density are important design constraints, as in avionics and space applications. Conventional IC packages are many times larger than the active chip inside. The typical 40-pin dual-in-line package has an area of about 1.0 square inches while the chip contained therein is typically 0.05 square inches. In hybrid assemblies, the substrate area required by each chip is comparable to the area of the chip itself, so that packing density (or functional density) is increased and weight is lowered by using hybrid technology.

A long-standing controversy has existed over the reliability of a hybrid microcircuit as compared to the same functional circuit implemented in standard PC technology. Many people in the industry appear to have preconceived notions as to the relative reliabilities of hybrids and PC functions. It appears that the hybrid should exhibit a reliability comparable to, or somewhat better than, the same function on a PC board.

This study has not specifically addressed this question, but the question has come up so many times that a thorough evaluation of the issue

4-3

will be presented here. The following salient points are relevant to the issue:

1. Neither IIT Research Institute nor any of the numerous individuals in other companies contacted during the course of this study possess any useful reliability data on both a hybrid function and the identical function fabricated on a PC board. If such data is available, we would be happy to see it.

2. There are numerous technical advantages to be realized by using a hybrid as compared to PC functions. These include smaller size weight, better thermal coupling, reduced parts count, etc.

3. There are some intuitively logical reasons why a hybrid might be less reliable than the equivalent discrete circuit. These include:

   o Semiconductor chips used in hybrids are difficult or impossible to test adequately in the hybrid. The discretely packaged devices on the PC assembly are much easier to test both before insertion and after insertion.

   o Hybrids are usually produced in small numbers, so that the benefits of a "learning curve" and of a mature process and/or line are seldom realized.

   o It is harder to perform accelerated testing on hybrids, since the hybrid can only be exposed to a stress which may be tolerated by the weakest component in the hybrid. With PC fabrication, each component can be individually tested to a stress level which will be effective in propagating failures.

   o Hybrid packaging and assembly techniques occasionally result in the occurrence of common-mode type failures and/or secondary failures which would not occur in the discretely fabricated version.

Thus, while we did not specifically address this controversy in the course of this study effort, we are of the opinion that our proposed model does represent a reasonable and accurate model for predicting the failure rate of hybrid microcircuits. No consideration whatsoever was given to how this might compare to the failure rate of the same function fabricated using PC technology.

4.1 Hybrid Model Development

Prior to the development of a new hybrid microcircuit reliability prediction model, a careful, thorough analysis of the existing model was performed. As a result of this analysis several specific deficiencies were identified, including;

o   model is tremendously complex

o   hybrid model is dependent on several other models, resulting in some "lack of control" of the model

o   accuracy of the hybrid model is poor

o   microwave hybrids are not addressed

o   non-hermetic hybrids are not addressed

Each of these points was addressed in the development of the final model. Microwave hybrids could not be addressed due to an almost total lack of data on these devices. (Additional problems with microwave hybrids were previously discussed in this report).

Also hampered by severe data shortages were non-hermetic hybrid assemblies. Fortunately, these devices are sufficiently similar in construction to non-hermetic monolithics as to permit some meaningful conclusions to be drawn. In the final model, there is a 2:1 ratio of failure rates for non-hermetic assemblies, as compared to an identical hermetic assembly. This is analogous to the microcircuit D-1 and D quality levels.

Of particular concern in the development of a new hybrid failure rate prediction model was the complexity issue. It was felt that the present approach of considering virtually every item in the hybrid-right down to the number of interconnects and the materials used may be too complex and that a simplified model may be used.

4-5

Considerable time was spent analyzing various device construction details in a search for a single useful measure of complexity. Multiple linear regressions were run against failure rate for a number of parameters, including number of IC's, transistors, diodes, resistors, capacitors, inductors, interconnects, substrate area, number of package pins, package seal perimeter, and total number of attached devices.

Results of this analysis were quite enlightening. It was found that the number of IC's, transistors, etc. had little impact on failure rate, after the number of interconnects had been fit into the regression. This is reasonably consistent with most published failure mode distributions for hybrids, which show interconnects as a major cause of failures. Further, there was no correlation at all between failure rate and the total number of parts of all types used in the hybrid.

Number of interconnects, N_I, was found to fit nicely in a regression model for the equation $\lambda = AN_I^\alpha$ were A and α are constants. (correlation coefficient was 0.58 when grouped, smoothed data were regressed). Thus a base failure rate λ_b for hybrids will be defined as

$$\lambda_b = 0.17N_I^{0.36}$$

This equation is valid up to at least 500 interconnects, the upper limit on devices in our database. (While this model does not distinguish between single metal and bi-metal bonds, it is recognized that single metal bonds are superior. Intermetallic growth is a problem with bi-metal interconnects and should be avoided whenever possible.)

An unexpected result of the exploratory data analysis performed was a high degree of negative correlation between failure rate and number of hybrids tested for any particular data record. Since number of devices on test is an apparently random, uncontrolled parameter this correlation was initially rejected as being spurious.

Later in the analysis it was discovered that the class of hybrids commonly referred to as "off-the-shelf" exhibited on the average, a failure rate approximately one tenth that of the class "custom hybrids". It was suggested that this improvement in reliability was attributable to reliability growth and/or a "learning curve" associated with the higher volume production of off-the-shelf hybrids.

As such an effect would not result in a step function, some time was spent in defining a continuous parameter π_L which would account for the learning curve associated with higher production volumes. This involved estimating the total number of hybrids produced for a number of specific hybrids in the database.

During the course of this analysis, it was realized that there was a high degree of correlation between the number of devices on test in a particular data record and the total number of devices produced - especially for custom hybrids used in military equipments. This would be consistent with the hypothesized correlation between failure rate and number of hybrids produced and would provide an acceptable explanation for the apparently spurious effect of number of hybrids on test on failure rate.

Since the number of devices produced could be determined for custom devices, but is seldom available for off-the-shelf (commercially available) hybrids, the factor π_L was defined to reflect these conditions.

Specifically:

$$\pi_L = \begin{cases} 84\ N_p^{-0.67} & \text{custom hybrids with } N_p < 5000 \\ 0.28 & \text{all off-the-shelf hybrids \& those custom hybrids with} \\ & \quad N_p \geq 5000 \end{cases}$$

4-7

where

N$_p$ = total number of hybrids produced

The π_L factor was defined so as to retain the 10:1 ratio of failure rates between custom and off-the-shelf hybrids contained in our database, as was previously discussed.

As with VLSI devices, the lack of a balanced database prevented the evaluation of the effects of environment and quality level on the failure rates of hybrids. What data could be found was therefore compared to existing microcircuit π_E values and existing hybrid π_Q values, to determine if any justification for changing these values could be found. As none was found, these π-factors were adopted as-is from the existing models.

In order to evaluate the effects of temperature on reliability it was necessary to use vendor life test data, as the available thermal information from field operating data was inadequate to support such an analysis. The normal Arrhenius relationship was assumed, and a linear regression was performed on the appropriately transformed data. This analysis indicated an equivalent activation energy of 0.32eV. This value is consistent with published literature and is in-line with activation energies for similar devices such as monolithic microcircuits. The temperature factor was thus defined as

$$\pi_T = 253 \times 10^3 \ \exp \ - \ (\frac{3708}{T_C + 273})$$

where T_C = case temperature of the hybrid (^oC)

The final hybrid microcircuit failure rate prediction model is given by

$$\lambda_p = \lambda_b \ \pi_E \ \pi_Q \ \pi_T \ \pi_L \ \pi_F \ \text{failures per } 10^6 \text{ hours}$$

4-8

where

λ_b is the base failure rate, as a function of the number of interconnects

π_E is the environmental factor

π_Q is the quality factor

π_T is the temperature dependent factor

π_L is the learning factor

π_F is the function factor

This model is presented in detail in Appendix A; Section 2 beginning on page A-16.

4.2 Hybrid Model Validation

To check the validity of the proposed hybrid model, predictions were performed on several devices for which field data were available. This work is summarized in Table 4.1. It can be seen that, with the exception of reference number 577, the prediction model corresponds very well to the actual observed failure rate. In fact, excluding this single line entry, the geometric mean of the ratio λ_p/λ_{obs} is 1.01. Failure rate predictions based on the existing hybrid microcircuit model in MIL-HDBK-217 are also presented for comparison purposes. The geometric mean of the ratio λ_p/λ_{obs} for the old model is 0.43.

TABLE 4.1: VALIDATION OF HYBRID MODEL

REF NO	τ_E	π_Q	π_F	π_T	λ_b	τ_L	λ_p (old)	λ_p (new)	λ_{OBS}	$\dfrac{\lambda_p(new)}{\lambda_{OBS}}$
515	2.5	1	1	1.49	1.14	5.7	3.96	6.78	7.63	0.88
514	2.5	1	1	1.49	1.23	5.7	4.83	7.31	6.14	1.19
513	2.5	1	1	1.49	1.13	5.7	4.10	6.72	6.14	1.09
512	2.5	1	1	1.49	1.15	5.7	3.98	6.84	10.75	.64
518	2.5	1	1	1.49	1.13	1.8	5.38	2.12	3.45	.61
520	2.5	1	1	1.49	1.08	6.3	4.47	7.10	5.17	1.37
519	2.5	1	1	1.49	.946	2.4	3.14	2.37	7.33	.32
517	2.5	1	1	1.49	1.02	5.7	5.38	6.06	9.22	.66
128	8.0	1	1	10.6	.49	1	.119	1.16	.730	1.59
127	8.0	1	1	10.6	.25	1	.012	.59	.330	1.79
577	4.0	1	1	2.18	.679	1	N/A	4.97	.301	16.51
167	7.0	1	1	3.69	1.31	2.4	N/A	22.7	21.3	1.07
257	8.0	1	1	10.6	.780	1.5	N/A	27.3	20.2	1.38
257	7.0	1	1	3.69	.780	3.9	N/A	22.0	10.4	2.12

5.0 VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)

5.1 Introduction

The VHSIC program is a Department of Defense program aimed at accelerating the development of complex, high speed integrated circuits specifically intended for use in military systems. Each of the six prime contractors are therefore responsible for developing "chip sets" whose functions are the most commonly needed in military system design. There is therefore a limited number of actual VHSIC chip types that will be produced.

The nature of the VHSIC program presents some unique problems in the development of a reliability prediction model. These problems will be discussed in more detail later.

The main objective of the VHSIC program is to increase the chip's Functional Throughput Rate (FTR). The FTR is defined as the number of equivalent gates times the operating frequency divided by the area of the chip, hence the unit Gate-Hz/cm^2. Since the FTR is the prime attribute to be maximized, the manner in which this is accomplished is through device scaling. The scaling of devices, along with its tremendous benefits to device operating characteristics, also may have adverse effects on device reliability. These effects will be further discussed in Section 5.2.

Phase I of the VHSIC program is being undertaken by six prime contractors whose efforts are aimed at developing 1.25 micrometer feature size chips with a FTR of 5 X 10^{11} Gate-Hz/cm^2. A summary of VHSIC chips is given in Table 5.1 (Reference 10).

TABLE 5.1: VHSIC CHIP SUMMARY

Contractor	Technology	Application	Functional Chips
Honeywell	Integrated Schottky Logic (ISL), Common Mode Logic (CML), (Both Bipolar)	Electro-optic Signal Processor	Parallel programmable Pipeline, Input Output Controller
Hughes	CMOS/SOS	AJ Communications	Digital Correlator Algebraic Encoder/ Decoder, Spread Spectrum Subsystem
IBM	NMOS	Acoustic Signal Processor	Complex Multiply and Accumulator
TI	Schottky TTL	Multimode-Fire and Forget Missile	Vector Arithmetic Logic Unit, Array Controller/Sequencer Vector address Generator, Multipath Switch Data Processor Unit, Device Interface Unit, General Buffer Unit
	NMOS		Static RAM
TRW	3D TTL (Triple Diffused TTL)	Electronic Warfare Signal Processor	Window Addressable Memory, Content Addressable Memory, Address Generator Matrix Switch Microcontroller Arithmetic Logic Unit Multiplier Accumulator
	CMOS		4-Port Memory
Westinghouse	CMOS/Bulk	Advanced Tactical Radar Processor	Pipeline Arithmetic Unit, 16 Bit Arithmetric Unit, Controller, 64 K Static Memory Exended Arithmetric Unit, Gate Array

In the past, the IC requirements of defense systems have been quite different than those which were commonly available in the commercial sector. This occurs for a number of reasons, one being the fact that commercial equipments inherently implement functions different than the high speed signal processing requirements of military electronics. Another reason is the fact that military systems often have size and weight constraints, indicating large scale integration is necessary. In many cases this requires a custom IC due to the lack of commercial availability, thus increasing systems costs while perhaps decreasing maintainability. Thus the implementation of VHSIC devices will eventually increase system performance, maintainability, and reliability, while ultimately reducing system cost.

Perhaps a fundamental driving force for VHSIC development is the overall system reliability which is achieved when increasing the level of integration on a single chip. This reduces the probability of failure due to the high failure rate failure modes, such as interconnects. In this study, factors that are considered during the design of the IC's will be addressed only with respect to how device reliability may be impacted.

Since these devices are much more complex than devices which have previously been used in military systems, testability is of great concern. The fact that testing every possible test vector is time prohibitive, much attention is being paid to the optimization of testing methodologies and the design of fault tolerant circuits. These factors, although not new are of major importance in VHSIC technology and again will be addressed in this report primarily on how they affect reliability.

VHSIC chips in actuality are "systems" and are being treated as such by VHSIC contractors with reliability tools such as Failure Mode and Effects Analysis (FMEA) conventionally used on systems now used at the chip level. In fact, several VHSIC contractors have indicated a desire to use a reliability prediction model suitable for use in designing and interfacing of various portions of chips, such as VHSIC's.

5-3

Since it is not possible at present to quantify a VHSIC reliability prediction model from empirical data, the remainder of this section of the report discusses areas of particular reliability concern which may influence a reliability prediction model. Specific attention is given to the effects of scaling and failure modes/mechanisms resulting from the reduced geometries. Also, fabrication techniques, testability/fault tolerance, radiation effects, and screening methods are discussed with an emphasis on how they impact device reliability and reliability predictions.

5.1.1 VHSIC Specifications and Goals

In the VHSIC program, there are requirements to meet minimum specifications. These specifications are of primary concern, especially in the areas of reliability and survivability. These concerns are of no less importance than the performance requirements (such as Functional Throughput Rate). Of particular interest is the tradeoffs between reliability, performance, and testability. Some major reliability requirements of the VHSIC program are as follows;

1) To achieve a failure rate of .006%/1000 hours at a 60% confidence limit for both operation and storage over the range of -55°C to +85°C case temperature. (After screening and burn-in).

2) Operate over the case temperature range of -55°C to 125°C.

3) Must operate in a radiation environment of 10^4 rads (Si) with a goal of 5×10^4 rads (Si).

4) Must operate after a transient radiation dose of at least 10^8 rads (Si)/s with a goal of 10^9 rads (Si)/s for a 10 nanosecond radiation pulse.

5) Must operate without permament damage after a neutron dose of at least 10^{11} neutrons/cm^2, 1 MeV equivalent.

Tradeoffs encountered between the achievement of these requirements and goals will be discussed further in subsequent sections.

5.2 Scaling Effects

Since the prime objective of the VHSIC program is to increase the functional throughput rate of the IC's, this means that the individual gate delays must be minimized, which in turn is accomplished by scaling the devices to very small geometries. By scaling device geometries, load capacitance is reduced and hence speed is increased. The scaling of integrated circuits, along with its tremendous benefits also may cause adverse effects which may impact device integrity and reliability.

Consider the scaling of a MOS transistor by a factor K. (that is K = old dimension/new dimension) (Ref. 2). As the oxide thickness, source and drain spacing, and channel width are scaled by the factor K, the doping density must increase by a factor of K and the gate voltage will decrease by a factor of K. General consequences of this scaling are;

1. device area decreases by K^{-2}
2. device delay times decrease by K^{-1}
3. Power dissipation decreased by K^{-2}
4. radiation hardness increased by K^{-2}
5. line resistances increase by K^2
6. current density increases by K
7. contact resistances increase by K^2

Numbers 1, 2, 3 and 4 are beneficial results of scaling and are indeed the reasons for the VHSIC scaling effort. Numbers 5, 6 and 7 however are adverse effects which must be carefully considered in the reliability assessment of these devices.

Another adverse effect of scaling which may affect reliability is the reduction in the signal to noise ratio by a factor of K^2. This effect

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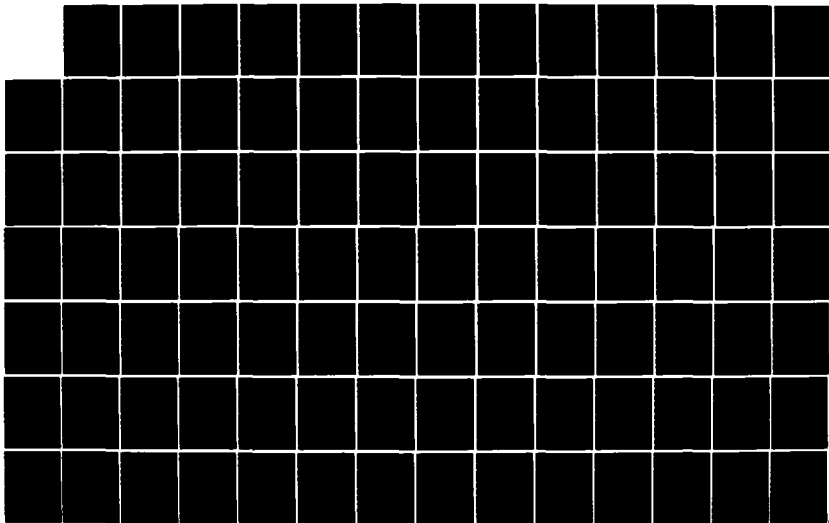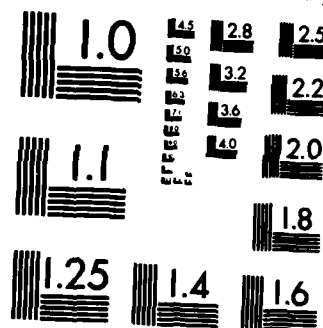
MICROCOPY RESOLUTION TEST CHART

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occurs since the RMS noise of a transistor decreases as the square root of the scaling factor, thus possibly making VHSIC more susceptible to thermally generated noise. Another such concern resulting from scaling is the radiation tolerance of small geometry components. Perhaps the single most important reliability concern from radiation is the threat of logic upset due to single particle disturbances, particularly alpha particles. It is clear that in general as device geometries are reduced, the susceptibility from alpha particle upset is increased. However, quantifying these effects is very difficult. Radiation effects will be discussed further in subsequent sections.

The submicron geometries encountered in the VHSIC program also present some unique problems in modeling device physics (Ref. 3). These problems are a result of the fact that the minimum feature size of VHSIC devices will be approaching the carrier mean free path. While some of the implications of this are known, others remain unknown and therefore more research is needed for a further understanding of submicron device physics and their possible reliability consequences.

Another scaling effect which has been noticed on the bipolar transistors is a degradation in gain when operated at very low current (i.e. less than 20 microamps). This may partially be due to the variation in the number of gates a particular transistor drives, making the driving capability of the transistor marginal in certain instances.

Possibly an important emerging aspect of VHSIC reliability due to scaling is the integrity of the metallization stripes. McAteer (Ref. 4) has indicated that the integrity of the metallization is particularly important at a neck down that occurs at an oxide step. Due to the smaller metallization widths and thicknesses the problem of detection by inspection becomes important, compounded by the fact that many VHSIC circuits have multilayer metallization structures. Since usual inspection of all metallization is no longer feasible, new techniques for insuring metallization integrity must be developed, or stripes prone to

electromigration type failures may become prevelant. Also, the current
inspection method of MIL-STD-883 does not account for thickness
variations, thus compounding the risk.

One alternative proceedure McAteer suggests is that a controlled
electrical pulse be applied to special test die metallization stripes. If
the metal line opens, the wafer metal is unacceptable, if not it is
acceptable. This method has several advantages, the main one of which is
the alleviation of the labor intensive method of MIL-STD-883.

The multiple layer structure presents several additional concerns and
potential failure mechanisms. The step metalization integrity just
discussed is aggravated with increasing step count and becomes most
compromised in the uppermost layer. Further, MOS devices employing
polysilicon in their fabrication are subject to a unique mechanism. The
integrity of the dielectric which interfaces with the polysilicon is in
question due to the tendency of polysilicon to nucleate into large grains
at the interface, causing disturbances at this interface.

Finally, scaling of the interconnect system may create new humidity
problems, namely, shorting across whisker growths between metallization
paths since the metal lines are now much closer.

In summary, the technique of scaling employed to achieve VHSIC
structures and functional performance properties, introduces some definite
reliability concerns that need to be addressed and resolved prior to
widespread application. These potential problem areas will play an
important role in establishing failure rate prediction factors and
variables.

5.3 Failure Modes and Mechanisms

The following sections deal specifically with failure modes and
mechanisms which can be expected in VHSIC devices. It is very important

to note that the degree of device scaling being utilized may lead to failure modes never before encountered in integrated circuits. It is for this reason that an accurate reliability prediction model will not be possible until VHSIC development advances to the point where valid empirical test data can be gathered which reflects these potentially new failure modes.

5.3.1 Electromigration

Electromigration is a mechanism by which mass is transported in a conductor under the influence of an electric field. The effect of this phenomenon can cause voids and hillocks along conductor paths, such as aluminum, causing opens or a shift in resistivity properties of the conductor.

This mechanism is a consequence of diffusion of metal atoms along the metallic grain boundries causing vacancies. Conversly, metal atoms coalesce to form hillocks. A factor that may contribute to electromigration is the thermal gradients formed in the material, causing a variation in the diffusion characteristics of the metal.

This effect may be particularly important in VHSIC metallization. As the cross sectional area of the metal lines decrease (increase in current density), there is an increase in I^2R heating, resulting in larger thermal gradients. Although currents are normally scaled along with the metallization widths, electromigration may be a problem at particular sites, such as steps where it is particularly difficult to get uniform metal coverage.

The importance of electromigration can be seen in the scaling laws. That is, as line widths are scaled by a factor proportional to K, the MTTF will become proportional to $1/K^5$ (assuming a constant current). The MTTF will be even lower at interconnection sites where larger thermal gradients can exist.

Although very preliminary data from VHSIC manufacturers indicate activation energies for electromigration may not be worse than for current VLSI technologies, it is a factor which must be carefully studied to insure the long term reliability of VHSIC devices. Texas Instruments (Ref. 15) has indicated that testing of 2.5 and 5.0 micron metallization yields an activation energy of .7 eV which is believed to be consistent with the .9 micron metallization which is to be used in VHSIC.

5.3.2 Hot Electrons

Another failure mechanism emerging with the advent of VLSI and hence VHSIC is that of hot electrons. A hot electron is an electron (or hole) which has sufficient kinetic energy to penetrate into, or even through the gate oxides of MOS structures, causing threshold shifts of the transistor or data losses in dynamic memories. Hot electrons can be generated from channel electrons which have gained energy from the channel field near the drain, carriers generated by impact ionization near the drain, or carriers which have been thermally generated by the substrate.

The generation of hot electrons is dependent on the channel length, width, gate oxide thickness, substrate doping, and applied voltages. Particular attention must be paid in the design of VHSIC devices to voltage scaling along with device geometry scaling to avoid high electric fields which contribute to the problem of hot electron generation. Since the gate oxide thickness of VHSIC devices will also be scaled to small dimensions, this will inherently increase their susceptibility to hot electron failures due to the increased probability that the hot electron will penetrate the oxide.

However, the substrate doping level is normally increased as devices are scaled. This results in a lower probability of failure due to the substrate leakage mode of hot electrons. It has also been noted however (Ref. 12) that for MOSFET devices hot electron failures will become less of a problem if constant electric field scaling is used. This is due to

the fact that the potential barrier does not change while the energy of the electron decreases due to voltage scaling.

5.3.3 Latch Up

Latch up is a phenomenon encountered in bulk CMOS circuits in which a parasitic NPNP bipolar structure can be triggered by externally applied energy into the latch up mode. This may be an important failure mode in VHSIC technology since six of the VHSIC devices are to be bulk CMOS.

This parasitic Silicon Controlled Rectifier, which when triggered (by externally applied voltage spikes, ionizing radiation, or high slew rate input pulses), causes a shunt path between the power supply and ground. This in turn results in localized heating possibly causing permanent chip failure. The device is inoperable in the latched state and remains in that state until the source is disconnected.

There are certain factors which influence the possibility of latch up, namely the current gain of the parasitic bipolar transistors, and the value of the parasitic resistance. If the gain of the transistors is greater than unity, the device may be susceptible to latch up. There are several design precautions that can be used to guard against latchup, one of which is to modify the biploar transistor current gain characteristics by altering the doping concentrations of the well. Another precaution is to implement the use of isolation between the bipolar elements. Also, since the parasitic resistances are a determining factor in latch up susceptibility, the resistivity of the well and substrate can be modified.

Although certain design rules can decrease susceptibility to latch up, scaling itself inherently increases the susceptibility to latch up. This is true in general since the gains of the bipolar parasitic transistors are dependent on their base widths, and the scaling of MOS transistors decreases this base width, hence increasing the gain. Also, the gain will increase as the well thickness decreases.

5-10

5.3.4 Oxide Breakdown

Another failure mode which will undoubtedly occur in VHSIC devices is oxide breakdown. Oxide breakdown is known to be one of the most frequently occurring failure modes of MOS large scale integrated circuits. This, coupled with the fact that the oxide thicknesses will be scaled (down to 100 angstroms) along with all other geometries in VHSIC devices makes it a particularly important reliability concern.

Oxide breakdown is typically the result of an applied voltage across the oxide. Low voltage breakdown has been correlated to oxide defects such as pinholes or irregular oxide thicknesses, indicating that these defects must be kept to a minimum if reliable VHSIC devices are to be realized. Defect densities are almost entirely process dependent and certainly will have to be closely monitored.

It has been shown that time dependent dielectric breakdown is associated with the accumulation of sodium atoms at the oxide silion interface, which are emitted from metal oxide interfaces. The fact that this mechanism can occur under relatively low oxide electric field strengths indicates it should be investigated further for its reliability implications. Also, the activation energy of oxide breakdown is low (typically .3 eV), indicating that although temperature may be somewhat effective in screening out these defects, it will be important to monitor and control these defects during device fabrication.

Along with the time dependent dielectric breakdown associated with oxide defects, the very thin oxides to be employed in VHSIC devices will make them much more susceptible to externally applied electrical overstress conditions from sources such as electrostatic discharge (ESD), electromagnetic interference, power supply transients, etc.

5.3.5 Electrostatic Discharge

As mentioned previously when discussing oxide breakdown, the very thin oxides to be used in VHSIC devices will make them susceptible to electrical overstress conditions such as electrostatic discharge. However, not only the oxides will be susceptible. The scaling of the devices has also increased the susceptibility of the bipolar structures as well by reducing the junction area and hence the power and current capabilities.

Although input protection will undoubtedly be incorporated on VHSICs, an ESD susceptibility mode may become prevelant that is not protected by the networks. This mode is known as the charged device susceptibility mode (Ref. 7). Historically, modeling of electrostatic discharge to ICs has considered an externally applied voltage transient from a charged source (capacitance) and discharged into a device (with one or more of its pins grounded) through a resistance. By modeling a discharge in such a way, an on-chip protection network can be incorporated that will clamp the transient voltage and hence absorb the energy contained in the transient before it can damage the more susceptible internal components of the circuit. In the charged device susceptibility mode, however, the transient is not from an external source. Consider a device being slowly charged via its inherent capacitance to ground (i.e. the device is electrically floating) and then one of its pins is suddenly grounded (by contacting any real or phantom ground plane). A very high amplitude, short duration pulse will result. Since the charge is stored on the device itself, the input protection will not necessarily limit the voltage as it was intended. Indeed, it has been shown (Ref. 7) that devices subjected to this type of discharge have been damaged at internal nodes and not at the periphery of the chip, which is normally the case from an externally applied transient.

Since the potential for damage from the charged device is directly proportional to the amount of charge a device can hold, it is evident that

5-12

the parameter of particular interest is the inherent device capacitance to a ground plane. In general it has also been shown that large scale integrated circuits with large die and lead frames are more susceptible due to their large geometries and hence large capacitance. This will be of particular interest to VHSIC devices since they will necessarily be of relatively large physical dimensions. Although the lead frame capacitance of VHSIC devices may be kept to a minimum by the use of leadless chip carriers and pin grid arrays, precautions must be taken to insure these devices are not subjected to transient electrical overstress.

The long term reliability of devices that have been exposed to a noncatastrophic transient is questionable. There have been studies (Ref. 8, 9) suggesting that these devices may exhibit higher failure rates than if never exposed to a transient. Although there is a lack of definitive data in this area, it is important to limit the possibility of VHSICs being degraded by transient electrical overstress.

VHSIC contractors are continuing studies on electrical overstress input protection networks to be used in VHSIC devices, with varying degrees of success.

5.3.6 Interconnects

Interconnects will be an important aspect of reliability, due to the large number of them to be used in VHSIC devices. In general, as more devices are integrated on a chip, a higher percentage of the chips area will be occupied by interconnects. Interconnects are prone to failure from electromigration, whisker formation, faulty ohmic contacts, and masking faults. Due to the possibility of whisker formation, and a host of other reasons, VHSIC circuits may be more susceptible to moisture related problems.

5-13

5.3.7 Electrical Bonds

A technique being considered for electrical connection bonds of VHSICs is solder bumps. This technique will have to be closely monitored since it has been noted that they are susceptible to fatigue from mechanical stress. It is evident that electrical bonds will be a prime reliability concern, since not only are the bonds going to be smaller but there will be a much larger number of them.

5.4 Fabrication Techniques

Due to the reduced geometries of VHSIC technology, it was necessary in the early phases of the VHSIC program to research lithography methods for circuit definition. This was true especially for the second phase of the program, which requires VHSIC feature sizes to be decreased from the 1.25 micrometer Phase I requirement to .5 microns.

To achieve the necessary resolution, techniques other than conventional optical lithography such as X ray, or electron beam (E-beam) lithography are necessary. Of particular importance in advanced lithography techniques is the resolution of the process and the registration accuracy, thus making the lithographic system itself very complex. The predominant lithography methods to be used in VHSIC production is currently E-beam. Any degree of misregistration, particularly for multilevel circuits, will adversely affect both yield and reliability.

One alternative for lithography being investigated is holographic lithography (Ref. 5). Although it is in early developmental stages, it offers many advantages such as the fact that particulate contaminants during wafer printing are not a problem due to the inherent process associated with laser holography.

Electron beam lithography can exhibit a much higher degree of resolution due to the fact that the degree of resolution is not limited by light diffraction as in the case of optical lithography. Rather, it is dependent on electron scattering and the limitations of the resist material itself.

The extreme scaling of VHSIC devices has also necessitated the use of high diffusion concentrations. This makes the purity of the basic materials an important reliability concern, since any impurities can result in dislocations and defects in the crystal structure, or localized resistivity fluctuations.

One VHSIC contractor has indicated that although the purity level of the basic starting material is not guaranteed by the vendor to meet adequate requirements, there haven't been major problems as a result of this impurity level.

This indicates that new tests are needed to monitor and control the level of impurities. Work is being done on SEM and EDAX evaluations, while the use of test chips for this purpose is also possible.

It has also been observed that the dry etching process which is to be widely used in VHSIC fabrication uses a chlorine based gas which may present corrosion problems from crystaline defects that result. This may be a possible source of latent defects.

Another possible adverse consequence of extreme device scaling is stray particle contamination during device fabrication. Clean rooms down to class 10 will be used to fabricate VHSIC devices which can have as many as 10 particles per cubic foot of air. The problem arises from the fact that oxide thicknesses of VHSIC devices are approaching the diameter of the minimum size particle that can be effectively removed in clean room air filtration. A high density of 50 - 100 angstrom particles may exist in a class 10 clean room. These particles can cause a number of adverse

reliability effects such as a degradation in oxide integrity, dislocations in the crystaline structure, and stacking faults. Compounding the severity of this problem is the fact that the airborne particles can be electrostatically attracted to the wafer during fabrication. This occurs since many of the materials used in a clean rooms are electrostatically charged quite easily and that many of the airborne particles themselves are charged.

The use of new materials may also have an impact on VHSIC reliability. For example, polyimide is being considered for use as a dielectric between the multiple layers of metallization. Since polyimide inherently has rounded edges, the step coverage can be improved with its use. It also improves the alpha particle absorption between layers. However, it also may have some adverse reliability effects such as long term instability since it is an organic material. Also, due to its hydroscopic nature, any water vapor present would cause it to expand and thus possibly set up mechanical stresses.

5.5 Testability/Fault Tolerance

Due to the extreme complexity of VHSIC devices, it has become necessary to incorporate elaborate built-in testing (BIT) schemes to insure the device is operating as required. This has prompted a major effort, known as DAST (Design Architecture, Software and Test), to be undertaken to research the subject. It is considered important enough to devote chip real estate to testing functions, thus increasing the chip complexity and size, and possibly effecting reliability. However, it should be noted that in the Phase I study of this modeling effort it was shown that increasing the device complexity does not necessarily increase the failure rate significantly.

Along with built-in testing schemes, fault tolerant (FT) designs are also to be incorporated in VHSIC designs. As in the case of BIT, the implementation of the fault tolerant design results in an increase in

circuit complexity. A fault tolerant IC, although experiencing a physical failure, will not be detected at the system level. This effect of BIT and FT, although directly affecting the chip failure rate, will be very difficult to quantitatively ascertain for reliability modeling purposes. These effects will however be incorporated in the base failure rate when empirical reliability data becomes available.

The reliability implication of fault tolerant designs must be more carefully studied. Empirical data will be necessary to quantitatively ascertain its importance, since many variables need to be investigated in the implementation of BIT/FT such as different approaches, different technologies, different functions, etc.

5.6 Radiation Effects

One of the prime objectives in the VHSIC program is to make the devices relatively immune to certain levels and types of radiation (total dose, burst, neutron, and single particle). The minimum requirements are as previously stated: 1) must operate without failure in a radiation environment of 10^4 rads (Si) 2) must operate without failure after a transient radiation dose of 10^8 rads (Si) for a 10 nanosecond radiaton pulse, 3) must operate without transient upset through a radiation pulse of 10^7 rads (Si) for a 10 nanosecond pulse duration and 4) must operate without permanent damage after a neutron dose of 10^{11} neutrons per cm^2, MeV equivalent.

5.6.1 Total Dose Hardness

Adding to the concern of total dose radiation tolerance is the fact
that MOS or CMOS technologies, which are inherently more susceptible to
radiation upset or failure are expected to predominate in the VHSIC
program. Eleven of the twenty eight VHSIC chips are to be of MOS
technology. MOS devices are more susceptible because that they operate
via surface effects. The primary effect of ionizing radiation is a
disturbance in the interface states at the oxide layers at the surface of
a device, causing a shift in threshold logic. Bipolar devices are not as
susceptible to total dose radiation as MOS structures since they depend on
bulk effects rather than surface effects.

Another failure mode associated with dose radiation is the latch up
effect observed in CMOS devices. As discussed previously this may be
important in the VHSIC program since many of the VHSIC devices are to be
CMOS.

5.6.2 Transient Radiation Hardness

Transient radiation is of the same type as total dose (gamma), but is
of a transient nature, with pulses typically less than one microsecond.
As in total dose, MOS structures are in general more susceptible than
bipolar with the failure mechanisms being the same.

5.6.3 Single Event Upsets

Due to the relatively small geometries encountered in VLSI technology,
new failure modes have appeared from sources such as neutrons, cosmic rays
and alpha particles. VHSIC technology is such that a single particle has
sufficient energy to cause a logic upset due to the relatively low amount
of charge stored at a capacitive node. Of particular interest in this
respect is alpha particles, since they are generated by the radioactive
decay of trace materials commonly found in IC package materials.

Problems associated with these single particle upsets are normally considered "soft errors" in that a permanent circuit fault is not encountered but rather a non-repeatable logic error is observed.

The sequence by which an alpha particle induced software error occurs is the following; an alpha particle penetrates the silicon surface of the semiconductor die and electron-hole pairs are generated. The total number of electron-hole pairs generated is dependent upon the energy of the incident particle. Next, electrons (for an n-channel device) or holes (for p-channel device) are collected at dynamic nodes via the electric fields, with the additonal net charge at that node possibly causing a change of state.

This may be a particularly important aspect of VHSIC reliability since:

1) the materials generating alpha particles (uranium and thorium) are commonly found in packaging materials to be used in VHSIC fabrication.

2) RAMS which will be widely used in VHSIC chips are particularly susceptible to alpha induced upset.

Materials in which uranium and thorium (and hence alpha particles) are found are ceramics, forms of glass, aluminum, molybdinum, and tungsten. Solder is also known to emit alpha particles. Since VHSIC devices will be packaged predominantly in ceramic and glass materials, precautions must be taken such as coating the chip surface with a polymer. Additionally, the effects of soft errors may be minimized by variations in the fabrication process designs by insuring that the amount of stored charge is high compared to the charge potentially induced by the alpha particle. This can be accomplished in a number of ways: 1) by implementing vertical capacitor plates, 2) by using an epitaxial layer or a buried n+ grid to absorb generated carriers, 3) by reducing the areas of floating (n+) regions, and 4) by careful layout of memory cell patterns. Unfortunately, such remedies are not effective in protecting the active elements from

alphas emanating from the chip material itself (i.e. aluminum). The only alternative to prevent this is to increase the purity of the starting materials, which is precisely the action being attempted by the VHSIC manufacturers. Also, a design approach being taken in VHSIC devices which will help alleviate soft error problems is the implementation of fault tolerant designs via redundancy, parity bits or similar techniques.

5.6.4 Neutron Hardness

Neutron radiation reduces the current gain of bipolar transistors by decreasing the minority carrier lifetime. Because of this phenomenon, bipolar devices are generally more susceptible to this kind of radiation than MOS devices. (Recall that MOS devices are majority carrier controlled devices.)

It must also be noted that the methods of lithography to be used in the manufacture of VHSIC devices (namely electron beam) may, inherently, adversely effect radiation hardness of the devices. This occurs since the lithography process itself exposes the device to a degree of radiation. The resulting damage is annealed after exposure, but unfortunately makes the device more susceptible to failure from subsequent radiation exposure. Preliminary results from Chen (6) indicate that devices fabricated using E-beam lithography as opposed to photolithography are more susceptible to radiation damage.

The mechanism believed to be occurring here is that the electron beam direct-write process creates neutral traps in gate oxides. It has been shown that these traps remain in the gate oxide after high temperature annealing, thus capturing hot electrons during device operation and degrading circuit performance (See also Section 5.3.2). It has also been shown that this effect is accelerated by exposure to radiation.

There are also some aspects of scaling which will indirectly increase the radiation hardness of VHSIC devices. The mandatory increase in the

quality of the silicon itself, along with the increase in the quality of the IC fabrication process controls, can reduce contamination and hence the susceptibility to radiation damage.

Andrews (Ref. 1) has shown that there is a rapid increase in the flux of heavy ions (cosmic) above an altitude of 40,000 feet. Since VHSIC components will be in aircraft operating above that altitude, and hence inherently susceptible to various levels of radiation, it is suggested that emperical data be analyzed, as it becomes available, to determine the true effect of radiation at various altitudes on reliability. For reliability modeling purposes, the base failure rate should reflect the probability of failure due to radiation effects. Field reliability data is required in each application environment before this effect can be properly analyzed.

5.7 Packaging Effects

Of critical importance to the success of the VHSIC program is the development of adequate packaging techniques. The two main techniques to be used in VHSIC devices are pin grid arrays and chip carriers. An illustration of a typical chip mounting surface is shown in Figure 5.1.

Chip carriers, although offering a somewhat lower number of I/O pins than pin grid arrays, are being used by VHSIC contractors in the 148 and 196 leaded, 25-mil center versions.

Pin grid array (PGA) packages are constructed in a manner similar to the ceramic chip carrier except that the connections to the circuit board or substrate are made through pins throughout the area of the base of the PGA, making them a good choice for high pin count packages. For VHSIC devices, PGAs of up to 240 pins will be employed.

CAVITY

POST AREA

SEAL RING

BACK BOND

ORIENTATION
ASSEMBLY MARK
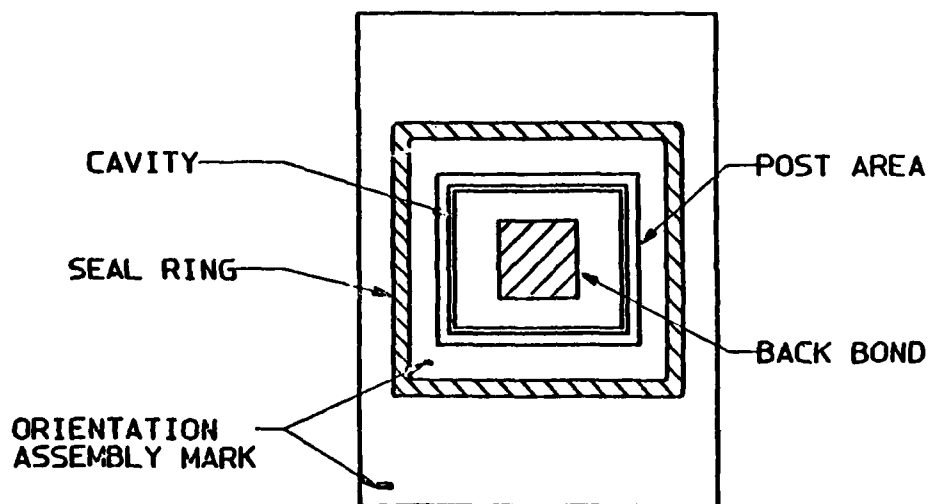
FIGURE 5.1: TOP OF SUBSTRATE

Since operating temperature is one of the most critical attributes affecting reliability, it is absolutely essential that sufficient chip cooling precautions be taken to assure adequate power dissipation. The power of VHSIC chips (typically 1-2 watts) is going to be such that low thermal resistances are needed. Preliminary data from VHSIC contractors has indicated typical junction to case thermal resistances of 1.0 - 3.5 ^{o}C/W for a device in a ceramic package.

5.8 Screening Methods

Since reliability is an integral part of the VHSIC program, screening methodologies to be employed will be a primary concern. MIL-STD-883 procedures are applicable and will be utilized for VHSIC devices. These would include: internal visual, stabilization bake, temperature cyclinq, constant acceleration, burn-in, final electrical, quality conformance inspection, external visual, and electrostatic discharge protection tests.

Due to many new factors in VHSIC technology, all screening methods which ultimately affect reliability must be examined for their applicability and effectiveness. One which deserves attention is the precap visual test. This test is becoming impractical due to the size and complexity of VHSICs. Alternative approaches (such as those contained in MIL-STD-883B method 5004, Paragraph 3.3.1 and 3.3.2) utilize stress testing to detect the faults which in the past have been detected visually. Computer aided optical systems which compare the chip under test to an image of a known good chip may also be alternatives.

As mentioned previously, new methods of detecting impurities and defects such as oxide defects or crystaline defects may be needed since these kinds of flaws impact the long term reliability of small scale devices more than they have in the past with larger geometry technology.

One possible approach for additional reliability evaluation is the use of test die data. VHSIC wafers must necessarily incorporate test die to monitor and control the fabrication processes. Test die are included on the wafer to control alignment, etch control/size control, metal control, and oxide control. The manner in which test die can be utilized to determine long term reliability is not yet quantified although they can be used to monitor parameters pertinent to reliability such as contact resistance, surface resistivity, bulk resistivity, metal line integrity, via integrity, dielectric integrity (thickness and pinhole density).

5.9 Problems Associated with Modeling VHSIC Reliability

VHSIC devices are unique to the development of reliability prediction methodologies for the following reasons:

1. The VHSIC program is intended to make a set of integrated circuits available that are the most common functions used in military equipment. There is therefore only a limited number of circuits to be made available and not a "technology" on which reliability prediction models are normally based.

2. Since VHSIC's are to be developed soley for military applications, reliability is intended to be an integral part of the design and fabrication processes, thus making the extrapolation of reliability factors of devices designed primarily for the commercial sector questionable.

3. VHSIC technology in many respects is new and unknown failure mechanisms may appear making reliability predictions impractical until these potential failure mechanisms can be identified and understood.

5.10 Proposed VHSIC Reliability Model Form

Since a quantitative reliability prediction model for VHSIC devices is not possible at this time, a model form is proposed which is believed to contain factors for all pertinent reliability attributes. When data is available for analysis, these factors can be tested for their impact on reliability and then quantified if found to be applicable.

5-24

The following VHSIC model is therefore proposed:

$$\lambda_p = \lambda_b \; \pi_C \; \pi_E \; \pi_p \; \pi_Q$$

where

  λ_b = base failure rate (based on device technology and junction temperature)

  π_C = device complexity factor

  π_E = application environment factor

  π_p = package complexity factor

  π_Q = quality level factor

The predicted failure rate is obtained by determining the appropriate base failure rate and multiplication factors.

Base Failure Rate (λ_b)

The base failure rate (λ_b) was made a function of the device technology and the case operating temperature. Since VHSIC devices are to be of many different technologies, one reliability prediction model whose base failure rate is a function of the technology is in order. Also, since the operating temperature is probably the single most important attribute affecting reliability, it was decided to incorporate this effect into the base failure rate. The effect which technology and case operating temperature have on failure rate is strongly related. A base failure rate equation dependent on both technology and temperature is, therefore, the recommended form for a VHSIC failure rate prediction model. Since each technology has its own normalization constants and equilavent activation energies in the Arrhenius relationship, these constants and activation energies will have to be determined from analysis of empirical data. VHSIC technology is anticipated to follow the Arrhenius relationship which relates failure rate to device activation energy and

5-25

junction operating temperature. The Arrhenius relationship has been
observed to accurately characterize the temperature dependence of
microcircuits. A discussion of the Arrhenius relationship as it relates
to component failure rate estimation is included in Section 6.2 "Analog
Microprocessor Failure Rate Model Development," of this report. The
Arrhenius relationship is as follows;

$$\lambda_b = A\ e^{-\frac{\varepsilon_{ea}}{k}}\ (\frac{1}{T_J} - \frac{1}{T_r})$$

where

A   = normalization constant for a specific technology

ε_{ea} = equivalent activation energy (as a function of technology)

k   = Boltzman's constant (8.63 X 10^{-5} eV/^{O}K)

T_J = junction temperature (^{O}K)

T_r = reference temperature (^{O}K)

Each VHSIC technology will have its own fixed A and ε_{ea} from which a
base failure rate can be determined. Once this is determined, the base
failure rate for a specific technology will be a function of only the
device junction temperature. The junction temperature can be calculated
by;

$$T_J = T_c + \theta_{Jc}P$$

where

T_J = junction temperature

θ_{Jc} = junction to case thermal resistance

P   = power dissipated

If failure rate data becomes available for various technologies at
various operating temperatures, it will be possible to empirically derive
equivalent activation energies to be used for failure rate prediction

of VHSIC devices. This activation energy will necessarily be from a composite of failure mechanisms but will be sufficient to develop an accurate temperature factor.

Data from Phase 1 of the study indicated that as device complexity increases, the failure rate approaches a constant value, or at least the failure rate increases much slower than the complexity. If this is verified for devices of VHSIC complexity, a device complexity factor may not be needed. Historically, complexity factors have been determined by the number of gates, transistors or bits. Although there is a relatively wide range of device complexities for VHSIC devices as measured by number of active devices, in many cases those numbers are not directly comparable due to the differences in fabrication technology.

Since the failure rate of complex microcircuits appears to be reaching an asymptotic value when measured against conventional complexity attributes (i.e. bits, gates, transistors), new approaches may be necessary to determine a complexity factor if one is considered necessary. Some possible attributes which may be used in determining a device complexity factor are:

1) The Functional Throughput Rate (FTR). (i.e. gate Hz/unit area)

2) The number of layers of interconnects.

3) Die size.

VHSIC contractors agree that a new measure of complexity may be required and that those mentioned above may represent possible alternatives. Certainly, all conventional measures of complexity and those mentioned above must be statistically analyzed against empirical data to quantitatively ascertain their usefulness as indicators of device reliability.

5-27

Application Environment (π_E)

Intuitively, it appears that application environment factors for VHSIC devices would be in the same proportion as the current microcircuit environment factors. Again, this would have to be verified by emperical data.

Package Complexity (π_D)

Due to the relatively new packaging techniques to be used in VHSIC devices, there is no historical experience that can be analyzed to determine the packaging effects. Currently, there is no available data on the package types and complexities to be used, namely leadless chip carriers and pin grid arrays of up to several hundred pins. Preliminary data from Phase I of the study indicated that observed failure rates for leadless chip carriers are statistically indistinguishable from side brazed ceramic DIP packages for lower complexity packages. However, there is no available data on side brazed ceramic DIPs of the complexities found in VHSIC.

Quality Level (π_Q)

Intuitively, it is reasonable to suggest that the quality factor as it appears in current microcircuit models would be applicable to VHSIC devices. The main difference, however, is that of VHSIC devices will be limited to the higher quality parts. No commercial quality VHSIC parts are anticipated, indicating that a new quality factor may be in order. Regardless of whether the current multiplication factors for quality are kept, they must be validated from empirical reliability data.

6.0 ANALOG MICROPROCESSOR

6.1 Device Description

For this study, an analog microprocessor was considered to be any digital microprocessor with on chip circuitry capable of accepting or outputting an analog signal. This is accomplished by means of integrating analog to digital (A/D) and/or digital to analog (D/A) functions on the same chip as a digital microprocessor. With these devices, an analog signal is converted to digital which is then manipulated in the desired fashion by means of the appropriate digital control signals.

Since the intent of this study was to develop a reliability prediction model for microprocessors with analog circuitry, a list of devices that fit this description were identified during the data collection task (Section 2.1.3.2) and are described in greater detail in Table 6.1.

"True" analog microprocessors, such as the Intel 2920 can be placed directly in the path of an analog signal by means of incorporating both A/D and D/A functions on chip. Of course, even these devices need the appropriate software for the necessary digital processing.

The AMI 2811, although often considered an analog microprocessor, does not have on-chip A/D or D/A conversion capabilities but instead depends on external components for these functions. Hence, the 2811 is actually a digital microprocessor specifically designed to manipulate digital signals from off-chip A/D converters.

The scope of this study encompassed a broad interpretation of the term "analog microprocessor" because of the following reasons.

1) The apparent ambiguity in the definition of analog microprocessors.

6-1

2) If an analog microprocessor is to be considered only a signal processor capable of being inserted directly in the path of an analog signal, then very few devices would qualify. Thus, a prediction model on these devices would be too narrow in scope and not allow for the prediction of the majority of devices listed in Table 6.1.

3) Because of the extremely limited number of devices considered true analog microprocessors, the amount of reliability data available for analysis would be prohibitively limited.

TABLE 6.1: ANALOG MICROPROCESSOR IDENTIFICATION

4-bit Microprocessor

Part Number	Technology	Analog Function	Notes
TMS 2100	PMOS	1-8 bit A/D	
TMS 2170	PMOS	1-8 bit A/D	
TMS 2300	PMOS	2-8 bit A/D	
TMS 2370	PMOS	2-8 bit A/D	
TMS 2400	PMOS	1-8 bit A/D	
TMS 2470	PMOS	1-8 bit A/D	
TMS 2600	PMOS	4-8 bit A/D	
TMS 2670	PMOS	4-8 bit A/D	
HD 4470	CMOS	2-5 bit A/D	
MB 88411	NMOS	1-8 bit A/D	
MB 88413	NMOS	1-8 bit A/D	
MB 88535	CMOS	1-6 bit 3-channel D/A	
MB 88536	CMOS	1-6 bit 3-channel & 1-13 bit D/A	

8-Bit Microprocessor

Part Number	Technology	Analog Function	Notes
S2200	NMOS	1-8 bit D/A & A/D	"A" Version UF Driver
S2210	CMOS	1-8 bit D/A & A/D	CMOS version
S2220	NMOS	1-8 bit D/A & A/D	µP compatible Data Bus
S2400	NMOS	1-8 bit D/A & A/D	"A" Version UF Driver
HD63L05	CMOS	1-8 bit A/D	LCD Driver
HD6805W0	NMOS	1-8 bit A/D	
MC6805R2	NMOS	1-8 bit A/D	
MC6805R3	NMOS	1-8 bit 4-channel A/D	
8022	NMOS	1-8 bit A/D	
µPD 8022	NMOS	1-8 bit A/D	
MC68705R3	NMOS	1-8 bit 4-channel A/D 3.7k EPROM	

Signal Processors

Part Number	Technology	Analog Function	Notes
2920	NMOS	1-8 bit A/D & D/A	25-bit Data Path
2921	NMOS	1-8 bit A/D & D/A	25-bit Data Path

There are certain problems associated with the implementation of analog to digital converters on an LSI microprocessor die. One 'is the fact that it is difficult to incorporate the A to D conversion with great accuracy due to the geometrical constraints of the small geometry components (resistor networks, comparators, etc.) This makes the analog to digital converter more sensitive to parametric drift from localized heat dissipation. In turn, the accuracy of A to D's normally implemented on microprocessors is lower than a comparable single chip A to D converter (2 LSB error compared to .5 to 1 LSB error). Although failures in the analog portion (of analog microprocessors) due to this effect may not be catastrophic, it could result in a device not operating within its specified tolerances, and hence more prone to failure from subsequent stressing.

There is also a secondary reliability concern with the use of these devices. The analog portion of the circuit often needs filtering before and/or after the analog microprocessor. The implications of this are increased circuit cost and complexity, and hence decreased system reliability.

Although there are differences in the architecture of the digital portion of these analog microprocessors compared to their digital counterparts, they are, for reliability purposes very similar. That is, they both normally contain a chip memory, arithmetic logic units, instruction decoders, etc. Also, since they are very similar to digital microprocessors, their failure modes, mechanisms and failure rates of the digital portion are assumed to be very similar (due in part to the lack of definitive failure mode data on the analog microprocessors).

6.2 Failure Rate Prediction Model Development

The initial approach attempted for model development of analog microprocessors was to identify and quantify significant failure rate model parameters solely by analysis of the collected life test data (presented in Section 2, Table 2.6). This initial model development approach was unsuccessful for two reasons. First, the collected data sample did not contain a broad range of the independent variables which were believed to have a significant effect on device failure rate. In fact, each of the collected data entries were tested at the same ambient temperature, and all parts were screened to the same level. The impact of these variables could not be detected by statistical analysis unless diverse values had been represented in the data set. The second reason that this model development approach was unsuccessful was that the number of available data entries was not sufficient to identify and quantify any more than one, or possibly two independent variables. The failure rate of a device as complex as an analog microprocessor could not be accurately predicted by a model with only one, or even two model parameters. Alternate model development approaches were considered because of the failure of the initial approach to yield an acceptable failure rate prediction model.

One alternate model development approach which was attempted was to analyze the analog microprocessor data together with the digital microprocessor data available from the RAC database (presented in Reference 15). Stepwise multiple linear regression was then applied to the merged dataset to identify variables which significantly affect both analog and digital microprocessor failure rates, and to quantify the difference between analog and digital microprocessors. The results of the regression analysis indicated that temperature and device technology have a significant effect on failure rate for the microprocessor family. However, the relative difference in failure rate between analog and digital microprocessors could not be detected by this analysis. It was assumed that this was either a result of a severely imbalanced database,

6-4

or that the expected increase in failure rate caused by the addition of the analog circuitry was less than the statistical noise contained in the data.

The alternate approach which was implemented for analog microprocessor model development was based on a thorough analysis of device construction, a study of anticipated failure modes/mechanisms, inspection of the existing MIL-HDBK-217D failure rate prediction model for digital microprocessors (Section 5.1.2.3, MIL-HDBK-217D) and comparison with the available life test data. The proposed analog microprocessor failure rate prediction model is presented in Appendix B in a form compatible with MIL-HDBK-217D. The following paragraphs present a detailed description of the methodology used to derive this failure rate prediction model.

The first step in this model development approach was to hypothesize a model form. Efforts in this step were concentrated towards identification of variables which theoretically have an impact on failure rate. Physics of failure information, failure mode/mechanism information, and reliability assumptions based on part construction were the major inputs in the development of the preliminary model. No attempt was made at this stage of the model development process to determine the relationship between the independent variables. The preliminary model was determined to be, (f denotes a function):

$$\lambda_p = f(T_j, V_S, V_{DD}, N_g, N_p, S, H, E, t, m, P)$$

where

    λ_p = predicted analog microprocessor failure rate (failures/10^6 hours)

    T_j = junction temperature ($^\circ$C)

    V_S = operating supply voltage (volts)

    V_{DD} = maximum recommended supply voltage (volts)

    N_g = number of gates

N_p = number of functional pins

S = screening level

H = hermeticity

E = application environment

t = technology

m = device maturity

P = programming technique

The second step in this failure rate prediction model development process was to examine different relationships between the independent variables. Failure rate prediction model forms which were considered and examined for analog microprocessors include a multiplicative model, an additive model and a combination of the two forms. The optimal failure rate prediction model form was determined to be similar to the prediction model for digital microprocessors. This model form is a combination of the additive and multiplicative model forms. This determination was based on construction similarities between analog and digital microcircuits, and also the documented reliability characteristics of microcircuit devices in general. The available life test data did not identify any deficiencies with this assumption. The hypothesized model form was therefore determined to be the following equation; f_i denotes a function.

$$\lambda_p = \pi_Q \, \pi_A \left[C_1 \, \pi_T \, \pi_V \, \pi_{PT} + (C_2 + C_3)\pi_E \right] \pi_L$$

where

λ_p = analog microprocessor predicted failure rate (failures/10^6 hours)

π_Q = quality factor = f_1(screening, hermeticity)

π_A = analog signal factor = f_2(number of analog bits, input and outputs)

C_1, C_2 = circuit complexity failure rates = f_3(gate count, device type)

π_T = temperature factor = f_4(temperature, technology)

π_V = voltage derating stress factor = f_5(operating voltage, max. recommended voltage)

π_{PT} = programming technique factor = f_6(technology, programming technique)

C_3 = package complexity failure rate = f_7(number of pins, package type)

π_E = environmental factor = f_8(combined environmental stress from application environment)

π_L = learning factor = f_9(device maturity)

The nature of the available data does not allow for quantitative analyses of the quality factor, voltage derating factor, environmental factor and the device learning factor. All available data was similar with respect to these parameters. In each case it was concluded that the factor developed for digital microprocessors could also be applied to analog microprocessors without introducing significant error. This assumption was based on similarities between analog and digital microprocessors. Additionally, it should be noted that the same quality factor, voltage derating factor, environmental factor and device learning factor are applied to all monolithic microcircuit failure rate prediction models in MIL-HDBK-217D. The construction and reliability characteristic differences between analog and digital microprocessors are less pronounced than differences between other microcircuit part types where these factors theoretically apply. Therefore it was concluded that these assumptions were reasonable.

There were insufficient data to analyze the validity of the existing microprocessor relationships for circuit complexity failure rate and package complexity failure rate. The two circuit complexity failure rate parameters (C_1, C_2) are a function of device type and gate count. These factors were assumed to be applicable to analog microprocessors. The package complexity failure rate parameter (C_3) is given as a function of the number of functional pins and the package type. This factor was also assumed to be applicable to analog microprocessors. These assumptions

were also based on construction similarities between analog and digital microprocessors. Neither the available life test data or the failure mode/mechanism investigations indicate that these assumption are invalid.

The impact of junction temperature was determined to be the most significant variable affecting analog microprocessor failure rate. Most microcircuit failure mechanisms involve one or more physical or chemical processes which occur at a rate which is highly dependent on temperature. It was assumed that the Arrhenius model applies to the reaction rate of analog microprocessor failure mechanisms. The Arrhenius model is based on empirical data and predicts that the rate of a given reaction will be exponential with temperature. In general terms, the Arrhenius model is given by,

$$\text{Reaction Rate} \quad \alpha \quad \exp(-\epsilon_{ea}/KT)$$

where

ϵ_{ea} = activation energy (eV)

K = Boltzman's constant

  = 8.63×10^{-5} (eV/$^{\circ}$K)

T = temperature ($^{\circ}$K)

Every chemical and physical reaction has a unique activation energy associated with it. During the life of an analog microprocessor there are several such reactions proceeding simultaneously, each capable of causing a part failure. The combined effects of these different reactions result in an analog microprocessor failure rate which is very complex and not in accordance with the simple form of the Arrhenius model given previously. Considering each physical and chemical failure mechanism separately (and assuming each mechanism is independent), the failure rate for analog microprocessors would be:

$$\lambda_p \quad \alpha \quad \sum_{i=1}^{n} (-\epsilon_{eai}/KT)$$

6-8

where

λ_p = analog microprocessor failure rate

n   = number of failure mechanisms

ϵ_{eai} = activation energy of the ith failure mechanism

The relationship given above was determined to be too complex to meet the objectives of this study effort. Therefore, alternate relationships of device failure rate vs. temperature were explored. While technically incorrect, the activation energy Arrhenius relationship concept has been applied to microcircuit failure rates (instead of failure mechanism reaction rates) often enough (References 21 and 22) to warrant further investigation. It has been found that for general classes of components with similar failure mechanism distributions, the cumulative effects of the various reactions can be approximated by an Arrhenius model for a specified temperature range. Because of the documented accuracy of this approximation, it was concluded that the analog microprocessor failure rate can be predicted as a function of temperature by the Arrhenius relationship for the range of temperature values found during normal usage (-55°C to +125°C). It should be emphasized that at extreme high and low temperatures (not found during normal usage), the Arrhenius relationship will no longer accurately predict analog microprocessor failure rate.

The tendency to refer to an "activation energy" for a given component such as analog microprocessors is technically incorrect. However, use of this terminology is informative if understood. An "activation energy" for a component is equivalent to stating that the temperature dependent nature of the component is the same as a component failing due to only a single failure mechanism with the specified activation energy. The use of the Arrhenius model to predict the failure rate of a component can be a very useful and accurate tool. However, the limitations of this action must be fully understood.

Upper and lower estimates of equivalent activation energy for analog microprocessors were determined by inspection of the equivalent activation energies for purely analog and purely digital circuits. The probability of failure due to the digital and analog portions of an analog microprocessor were assumed to be independent. Therefore, mathematically, the equivalent activation energy approximation for analog microprocessors must lie somewhere between the relatively higher value for the analog portion of the circuit and the lower value for the digital portion. This is true because an analog microprocessor can be considered a "hybrid type" device composed of both analog and digital circuits. The following equations illustrate this relationship.

$$\lambda_p \ \alpha \ B_1 \ exp(-\epsilon_{a1}/KT) \simeq B_2 \ exp(-\epsilon_{a2}/KT) + B_3 \ exp(-\epsilon_{a3}/KT)$$

$$\epsilon_{a2} \leq \epsilon_{a1} \leq \epsilon_{a3}$$

where

λ_p	=	analog microprocessor failure rate
ϵ_{a1}	=	analog microprocessor equivalent activation energy
ϵ_{a2}	=	digital equivalent activation energy
ϵ_{a3}	=	analog equivalent activation energy
K	=	Boltzman's constant = 8.63×10^{-5} eV/°K
T	=	junction temperature (°K)
B_1, B_2, B_3	=	constants

Table 6.2 presents the equivalent activation energies which are currently applied to microcircuits in MIL-HDBK-217D. The microcircuit temperature factor normalization constant (constant A in Table 5.1.2.5-4; MIL-HDBK-217D) was multiplied by Boltzmans constant to calculate equivalent activation energy. Based on the information provided in Table 6.2, it was concluded that the equivalent activation energy for hermetic analog microprocessors is between 0.50 eV and 0.65 eV, and the equivalent

activation energy for nonhermetic analog microprocessors is between 0.70 eV and 0.90 eV.

TABLE 6.2: MICROCIRCUIT EQUIVALENT ACTIVATION ENERGIES

		Equivalent Activation Energies	
Circuit Type	Technology	Hermetic	Nonhermetic
Digital	PMOS	0.50	0.70
Digital	NMOS	0.55	0.80
Analog	bipolar l..near	0.65	0.90

All collected life test and burn-in data were for an ambient test temperature of 125°C. Thus, equivalent activation energies could not be determined empirically. After consideration of several different methods to determine equivalent activation energies for analog microprocessors, it was concluded that the existing MIL-HDBK-217D values for digital circuits could also be applied to analog microprocessors. This assumption was based on the fact that the lower equivalent activation energies for digital circuits (relative to analog circuits) result in a conservative approximation (i.e. predicts a slightly higher failure rate) for junction temperatures less than 125°C. It was felt that this conservative approximation was justified because of the limited supply of accurate analog microprocessor failure rate data.

The concept of a lower activation energy resulting in a higher predicted failure rate seems contrary to intuition, and therefore will be discussed further. The logarithm of the failure rate is linear with respect to the inverse of temperature according to the equivalent Arrhenius relationship. Therefore the equivalent activation energy is the slope of the line defined by the logarithm of failure rate as a function of inverse temperature. In equation form,

$$\lambda_p = A \exp(-\epsilon_{ea}/KT)$$

6-11

$$\ln(\lambda_p) = \ln A - \epsilon_{ea}(1/KT)$$

This relationship is shown for two different activation energies in Figure 6.1. The example depicted in Figure 6.1 is analogous to the study of activation energies for analog and digital microprocessors. The activation energy (E_{a1}) for the more temperature dependent failure rate is greater than the activation energy (E_{a2}) for the less temperature dependent failure rate, as would be expected. However, the failure rate is lower for the more temperature dependent relationship for all points to the right of the intersection point. It should also be noted that as temperature decreases, the (1/KT) term increases. Therefore in the example depicted in Figure 6.1, the failure rate is less for the E_{a1} activation energy relationship for all temperatures less than T_0 (i.e. to the right of the intersection point).
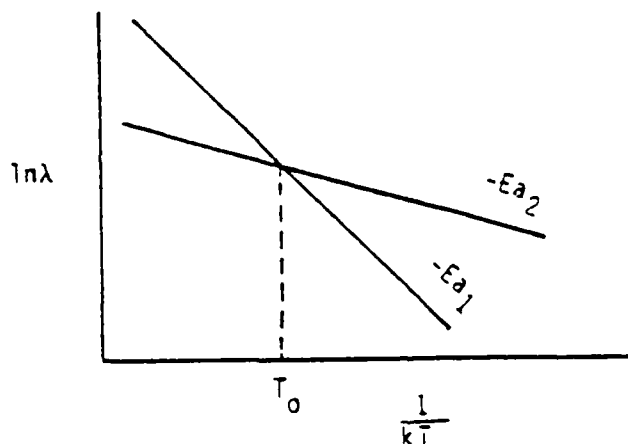
FIGURE 6.1: FAILURE RATE VS. TEMPERATURE

The temperature intersection point is 125°C for the analog microprocessor failure rate data. All collected life test and burn-in data was for a junction temperature slightly greater than the 125°C ambient test temperature. All potential failure rate prediction models based on the observed data will predict the same failure rates at 125°C regardless of the assumed equivalent activation energies. For

temperatures less than 125°C, a conservative failure rate estimate is thus provided by the relatively lower equivalent activation energies for digital circuits given in Table 6.2.

The requirement for a programming technique failure rate modifier was identified during the preliminary model development phase. It was assumed that the existing MIL-HDBK-217D microcircuit programming technique factor (Table 5.1.2.5-25 in MIL-HDBK-217D) was applicable to analog microprocessors. The existing factor is defined by the following relationship.

π_{PT} = 1.0, metal mask programming

π_{PT} = 0.985 + (9.5 x 10^{-5})(B), for bipolar PROMs utilizing NiCr, TiW, Polysilicon or Shorted Junction (AIM) Links

π_{PT} = 0.950 + (7.5 x 10^{-5})(B), for MOS PROMs, both UV and Electrically Erasable

where

π_{PT} = programming technique factor

B = number of bits

An analog signal factor was defined during the preliminary model development stage to be a function of the number of analog bits. This relationship could not be estimated for two reasons. First, only three of the nine collected life test data entries had observed failures. (Data is presented in Table 2.6 in Section 2 of this report). A precise measure of failure rate cannot be calculated without observed failures. For this reason, the required regression techniques could not be applied to define an analog signal factor as a function of analog bits. The second reason that this relationship could not be estimated was that the remaining three data entries were from burn-in testing. Failure rates calculated from burn-in data are assumed to include infant mortality failures, and therefore provide only an upper limit on failure rate. Again, proper

application of regression analysis requires that the dependent variable (i.e. failure rate) can be measured without error, and this is clearly not the case for zero failure data entries and burn-in data entries. Therefore, a modification of the preliminary model was required. The modified model includes an analog signal factor which is assigned a value of one for microprocessors without the presence of an analog signal and a constant value which is greater than one for analog microprocessors. It was concluded that a factor of this form could be quantified even with the inherent weaknesses included in the analog microprocessor database.

The process of determining an analog signal factor began by calculating a predicted failure rate (temporarily assigning the analog signal factor a value of one) for all part types where data was available. Table 6.3 presents the predicted failure rates and the input parameters used to compute the failure rates. The second step in the process was to compare the observed and predicted failure rates. Table 6.4 presents the observed point estimate failure rate, upper and lower 90% confidence limit values, and the predicted failure rates. A worst case point estimate failure rate was computed for zero failure data entries by assuming one failure.

TABLE 6.3: ANALOG MICROPROCESSOR PREDICTED FAILURE RATE

Data Entry	π_Q	π_T	π_V	π_{PT}	C_1	C_2	C_3	π_E	π_L	λ_{pre}
1*	17.5	13	1.0	1.0	.030	.0013	.014	.38	1.0	6.93
2*	17.5	13	1.0	1.0	.030	.0013	.024	.38	1.0	6.99
3*	17.5	13	1.0	1.0	.030	.0013	.014	.38	1.0	6.93
4*	17.5	13	1.0	1.0	.030	.0013	.024	.38	1.0	6.99
5*	17.5	22	1.0	1.0	.052	.0017	.024	.38	1.0	20.19
6, 7	17.5	22	1.0	1.0	.052	.0017	.024	.38	1.0	20.19
8	17.5	22	1.0	3.2	.053	.0017	.014	.38	1.0	65.40
9, 10	17.5	22	1.0	1.3	.028	.0012	.014	.38	1.0	14.12
11, 12	17.5	22	1.0	1.0	.028	.0012	.014	.38	1.0	10.88

* number of bits assumed to be 1,200

TABLE 6.4:   OBSERVED VS. PREDICTED FAILURE RATES

Data Entry	$\lambda_{.05}$	λ_{obs}	$\lambda_{.95}$	λ_{pred}
1	--	7.63*	22.90	6.93
2	--	7.63*	22.90	6.99
3	--	7.58*	22.70	6.93
4	--	7.58*	22.70	6.99
5	0.30	5.83	27.70	20.19
6	41.10	231.00	729.00	20.19
7	--	9.92*	29.70	20.19
8	--	44.09*	132.00	65.40
9	6.54	36.80	116.00	14.12
10	0.05	0.95	4.51	14.12
11	--	23.15*	69.30	10.88
12	0.27	1.51	4.73	10.88

* one failure assumed

The information provided in Table 6.4 was scrutinized to identify any inconsistencies.   Ten of the twelve data entries did not indicate any discrepancies with stated assumptions.   These data entries (1-9, 11) either had an observed failure rate greater than the predicted failure rate, or the predicted failure rate was within the 90% chi-squared interval.   This was considered to be an encouraging sign because of the uncertainties regarding failure rate estimation.   It must be remembered that the failure rate predictions were performed assuming an analog signal factor of one, which corresponds to a digital microprocessor.   Therefore it was anticipated that the observed failure rates would be greater than the predicted failure rates because of inherent reliability differences between analog and digital signals.   The two remaining data entries (10, 12) had predicted failure rates which were greater than the upper 95% confidence limit.   Device physics indicate analog microprocessors will not be more reliable than digital microprocessors and therefore that data entries 10 and 12 were not representative of analog microprocessors. These data points were therefore deleted from subsequent analysis.   It should be noted that the predicted failure rate for data entry #6 is below the lower 5% confidence limit.   However, it was anticipated that the

observed failure rates would be higher than the predicted failure rates, and therefore data entry #6 was not eliminated from the analysis. It would be expected that 5% of all data entries would lie outside the 90% confidence interval to either side, and therefore perhaps one data entry can be expected to be a natural outlier. Possible explanations for having two outliers are poor data recording practices or an application environment not typical of a test environment.

The geometric mean of the observed failure rates divided by the predicted failure rate was calculated for the ten data entries which were assumed to be typical of analog microprocessors. This calculation was performed to derive an analog signal factor for analog microprocessors. The calculation resulted in the following analog signal factor to be applied to microprocessors.

π_A = 1.0, digital microprocessors
π_A = 1.24, analog microprocessors

The derived analog signal factor was based on only limited data resources. However, the data analysis task was supplemented by thorough analyses of part construction and anticipated failure modes and mechanisms. It was concluded by these analyses that the derived analog signal factor properly discriminates against known reliability characteristics, and that the magnitude of the factor appears to be in agreement with theoretical reliability considerations.

Derivation of the analog signal factor concluded the failure rate model development for analog microprocessors. The proposed model properly discriminates against application and environmental variables which were assumed have a significant effect on device failure rate. The proposed model was based primarily on assumptions concerning similarities between analog microprocessors and other types of microcircuits. Therefore, the proposed model should be evaluated with field experience data and additional life test data when the data becomes available.

6-16

7.0 RECOMMENDATIONS AND CONCLUSIONS

7.1 Recommendations

It is recommended that the models developed as a result of this study be adopted in a future revision of MIL-HDBK-217. It is believed that these models represent a reasonable and accurate analysis of the reliability performance of VLSI, hybrid and analog microprocessors in actual field usage conditions. It is further believed that the module for VLSI and hybrid microcircuits represent a substantial improvement over the existing models in MIL-HDBK-217.

Previously no single acceptable source of failure rates was available for analog microprocessors. Their inclusion into MIL-HDBK-217 will allow for more consistent evaluations of reliability predictions, reliability trade-offs and life cycle cost analyses for equipments designed with analog microprocessors.

It is also recommended that RADC continue to study the reliability of VLSI devices over the next few years. This study was based on the necessarily sparse data accumulated during the first few years of VLSI technology. While statistically inconclusive, evidence was uncovered during the course of this study which would indicate a substantial reliability improvement in VLSI devices from 1977 to 1981 - perhaps as much as a factor of 5 improvement. For this reason it is important that the reliability of these devices be tracked over the next few years until such time as they may be regarded as a mature and stable product.

It is recommended that RADC support an effort dedicated solely to the collection and analysis of failure rate data on microwave hybrids. These hybrids represent a significant departure in technology from the conventional hybrid, and high-quality data on these devices is simply not available at the present time.

Since many of the yield enhancement/manufacturing technology efforts for VHSIC devices will be pursued in the 1984-86 time frame, it is evident that many of these efforts will impact reliability. Therefore it is strongly recommended that a reliability modeling effort be initiated at that time to provide a thorough analysis of VHSIC reliability. The results from this study can be used as a basis for future failure rate prediction models. It is also urged that every attempt be made to collect accurate life test and field experience data as it becomes available.

It was noted during this study that many of the part and equipment manufacturers were reluctant to furnish uncontracted data free of charge. This reluctance may be due to material and manpower costs incurred in providing the data, or due to the proprietary nature of the data. The study contractor is normally not provided with sufficient funds to allow for the purchase of these data. Therefore it is recommended that the government investigate methods for identifying, formatting and gaining access to data produced (as primary or secondary objective) under government funded contracts (e.g. the VHSIC program) and for storing the data in a central repository such as the Reliability Analysis Center, which is available to all government contractors. Additionally, the government provides funds for many part testing, maintenance support, life-cycle cost and reliability improvement warranty contracts which yield meaningful failure experience data. A centralized point such as GIDEP or the Reliability Analysis Center should be on automatic distribution to receive copies of the raw data collected during these contracts. These data would then be available for use in reliability studies such as the VLSI Device Reliability Models modeling effort.

Finally, it is suggested that the USAF and RADC closely scrutinize their maintenance data collection and reporting systems. Close coordination of the data needs of the reliability world with the types of information tracked and collected by the logistics world stands to reap tremendous benefits for both parties. A good deal of the time and effort invested in reliability programs is now lost due to inadequate or

7-2

incomplete documentation. It must be impressed upon program management and technical personnel that a complete, effective reliability program must include a validation and documentation phase. Documentation, preferably in the form of standard data items (DID's), must be made available to the DoD community if others are to benefit from the acquired knowledge and lessons learned.

7.2 Conclusions

It is concluded that the proposed failure rate prediction models for VLSI, hybrid, and analog microprocessor microcircuits represent accurate, technically sound models for the evaluation of anticipated field reliability performance for these devices.

It is also concluded that these models represent a substantial improvement over the existing models. For this reason it is proposed that these models be incorporated into a future revision of MIL-HDBK-217.

As has been discussed, the increase in complexity for VHSIC along with the smaller circuit dimensions have a direct impact on reliability. VHSIC devices are achieving levels of complexity comparable to entire systems, and therefore will have to be treated as such in the future. In particular, the area of fault tolerant design, which in the past has been implemented at the system level, is now being implemented at the chip level. This offers unique problems of reliability modeling which surely will have to be addressed. When actual field failure rates are obtained and analyzed for reliability modeling purposes, factors such as redundancy and fault tolerance must be considered and most likely will be inherent in the base failure rate.

Due to the fact that fabrication techniques are being developed for tighter tolerances, and reliability is now a design concern, most contractors at this point are optimistic about achieving the .006%/1000 hours reliability goal for VHSIC. However, this figure certainly must be

validated with empirical data due to many new reliability factors. It is clear that existing MIL-HDBK-217 models are inadequate for the prediction of VHSIC reliability.

Neither the proposed failure rate prediction model for analog microprocessors or the hypothesized model form for VHSIC are as sophisticated as was originally intended. This was entirely due to lack of sufficient data or lack of detail in the data. The reasons for these data deficiencies are:

o   VHSIC devices are in too early a stage of development for data to be available

o   Part types are low population devices

o   Data contributors are generally reluctant to incur any expenditure to further refine information they provide without charge

o   Potential data contributors are hesitant to allow visitors access to their proprietary databases.

Consequently, several factors considered for these two part type could not be included in the proposed models. Additionally, the factors that were included in the models had to be developed from existing MIL-HDBK-217 microcircuit models, or had to be developed by analytical methods other than direct analysis of field experience and life test data.

Appendix A

Replacement Pages for MIL-HDBK-217

Section 1: Proposed VLSI Failure Rate Prediction Model

Section 2: Proposed Hybrid Microcircuit Failure Rate Prediction Model

Section 3: Proposed Analog Microprocessor Failure
Rate Prediction Model

Appendix A

Section 1: Proposed VLSI Failure Rate Prediction Model

VLSI MOS and Bipolar Logic Devices with or without on-chip Memory (No. of Bits plus No. of Gates greater than 3000 and number of package pins less than 130).

Part operating failure rate model (λ_p):

$$\lambda_p = \pi_Q (0.0615\ \pi_T + C_3\ \pi_E)\pi_L \quad \text{Failures}/10^6 \text{ hours}$$

where

λ_p is the device failure rate in $F/10^6$ hours

π_Q is the device quality factor, Table 5.1.2.5-1

π_T is the temperature acceleration factor based on technology (Table 5.1.2.5-4) and is found in Tables 5.1.2.5-5 thru 5.1.2.5-13.

π_E is the application environment factor, Table 5.1.2.5-3

π_L is the device learning factor, Table 5.1.2.5-2

C_3 is the package complexity factor, Table 5.1.2.5-26

5.1.2.5 Tables for the Monolithic Model Parameters

TABLE-5.1.2.5-1. Π_Q, QUALITY FACTORS

Quality Level	Description	Π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements.	0.5
B	Procured in full accordance with MIL-M-38510, Class B requirements.	1.0
B-0	Procured in full accordance with MIL-M-38510, Class B requirements except that device is not listed on Qualified Products List (QPL). The device shall be tested to all the electrical requirements (parameters, conditions and limits) of the applicable MIL-M-38510 slash sheet. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D.	2.0
B-1	Procured to all the screening requirements of MIL-STD-883, Method 5004, Class B and in accordance with with electrical requirements of MIL-M-38510, DESC drawings, or vendor/contractor electrical parameters. the device shall be tested to all the quality conformance requirements of MIL-STD-883, Method 5005, Class B. No waivers are allowed except current and valid generic data** may be substituted for Groups C and D. This category applies to DESC drawings and contractor prepared specification control drawings (SCD's) containing the above B-1 screening and quality conformance requirements.	3.0
B-2	Procured to vendor's equivalent of the screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with the vendor's electrical parameters and vendor's equivalent quality conformance requirements of MIL-STD-883, Method 5005, Class B. Applies to contractor prepared SCD's containing the above B-2 screening and quality conformance requirements.	6.5
C	Procured in full accordance with MIL-M-38510, Class C requirements.	8.0
C-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class C and the qualification requirements of Method 5005, Class C. Generic data may be substituted for Groups C&D	13.0

TABLE-5.1.2.5-1. Π_Q, QUALITY FACTORS

Quality Level	Description	Π_Q
D	Hermetically sealed part with no screening beyond the manufacturer's regular quality assurance practices; parts encapsulated with organic material.*	17.5
D-1	Commercial (or non-mil standard) part, encapsulated or sealed with organic materials (e.g., epoxy, silicone or phenolic).	35.0

*All encapsulated devices must be subjected to 160 hr. burn-in at 125°C., 10 temperature cycles (-55°C to 125°C) with end point electricals, and high temperature continuity test at 100°C.

**Group C generic data must be on data codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process, and from the same plant as the die represented. Group D generic data must be on data codes no more than one year old and on the same package type (see 3.1.3.12 of MIL-M-38510) and from the same plant as the package represented.

TABLE 5.1.2.5-2: π_L, LEARNING FACTORS

The learning factor π_L is 10 under any of the following conditions:

(1) New device in initial production
(2) Where major changes in design or process have occurred.
(3) Where there has been an extended interruption in production or a change in line personnel (radical expansion).
(4) For all new and unproven technology such as CMOS fabricated on sapphire substrates (CMOS/SOS).

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as six months of continuous production.

π_L is equal to 1.0 under production conditions not stated in (1), (2) and (3) above.

TABLE 5.1.2.5-3: APPLICATION ENVIRONMENT FACTOR π_E

Environment	π_E	Environment	π_E
S_F	0.90	A_{IC}	2.5
G_B	0.38	A_{IT}	3
G_F	2.5	A_{IB}	5
N_{SB}	4.0	A_{IA}	4
N_S	4.0	A_{IF}	6
M_P	3.8	A_{UC}	3
G_M	4.2	A_{UT}	4
M_{FF}	3.9	A_{UB}	7.5
M_{FA}	5.4	A_{UA}	6
N_U	5.7	A_{UF}	9
N_H	5.9	U_{SL}	11.0
N_{UU}	6.3	M_L	13.0
A_{RW}	8.5	C_L	220.0

TABLE 5.1.2.5-4. TECHNOLOGY TEMPERATURE FACTOR TABLES
(SEE NOTES BELOW)

Technology	Package Type	Π_T Table Number	A
TTL, HTTL, DTL & ECL	Hermetic Nonhermetic	5.1.2.5-5 5.1.2.5-6	4635. 5214.
LTTL & STTL	Hermetic Nonhermetic	5.1.2.5-6 5.1.2.5-7	5214. 5794.
LSTTL	Hermetic Nonhermetic	5.1.2.5-7 5.1.2.5-8	5794. 6373.
IIL & MNOS	Hermetic Nonhermetic	5.1.2.5-9 5.1.2.5-12	6952. 9270.
PMOS	Hermetic Nonhermetic	5.1.2.5-7 5.1.2.5-11	5794. 8111.
NMOS & CCD	Hermetic Nonhermetic	5.1.2.5-8 5.1.2.5-12	6373. 9270.
CMOS, CMOS/SOS & Linear	Hermetic Nonhermetic	5.1.2.5-10 5.1.2.5-13	7532. 10429.

Note 1. $\Pi_T = 0.1e^x$

where $x = -A \left(\dfrac{1}{T_J + 273} - \dfrac{1}{298} \right)$

A = value from above Table

T_J = device worst case junction temperature (^{o}C).

e = natural logarithm base, 2.718

A-7

Proposed
MIL-HDBK-217X
MICROELECTRONIC DEVICES
MONOLITHIC

(Notes continued for Table 5.1.2.5-4)

NOTE 2. T_J, the worst case junction temperature, shall be measured or
estimated using the following expression:

$$T_J = T_C + \theta_{JC}P$$

where:

T_C is case temperature (^{O}C.).

θ_{JC} is junction to case thermal resistance (^{O}C/watt) for a device soldered
into a printed circuit board. If θ_{JC} is not available, use a value
contained in a specifiction for the closest equivalent device or
use the table below.

P   is the worst case power realized in a system application. If the
applied power is not available, use the maximum power dissipation
from the device specification or from the specification for the
closest equivalent device.

If T_C cannot be determined, use the following:

ENVIRO.	G_B	S_F	G_F	N_{SB}	N_S	M_P	G_M	M_{FF}	A_{IT}	M_{FA}	A_{IC}	A_{IA}	A_{IB}
T_C (^{O}C.)	35	40	45	45	45	40	50	60	60	50	60	60	60

ENVIRO.	N_U	A_{UT}	N_H	N_{UU}	A_{RW}	A_{IF}	U_{SL}	A_{UF}	M_L	C_L	A_{UC}	A_{UA}	A_{UB}
T_C (^{O}C.)	80	95	45	25	60	60	40	95	60	45	95	95	95

If θ_{JC} cannot be determined, use the following:

Package Type	Die Attach*	Number of Package Pins	
		$\leq$ 22 pins	> 22 pins
Leadless Chip Car-riers (LCCs)	Eutectic	30	25
Hermetic DIPs	Epoxy or Glass	125	100
Nonhermetic DIPs	Eutectic	30	25
	Epoxy or Glass	125	100
Hermetic Flatpacks	Eutectic	40	35
	Epoxy or Glass	125	100
Hermetic Cans	Eutectic	30	NA
	Epoxy or Glass	125	NA

* If the die attach method cannot be determined, assume that epoxy die attach is
used for hermetically packaged CMOS and eutectic die attach for all other her-
metic packages.

A-8

Table 5.1.2.5-5. π_T VS. JUNCTION TEMPERATURE FOR HERMETIC TTL, HTTL, DTL, & ECL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.35	77	1.0	103	2.5
27	0.11	53	0.38	79	1.1	105	2.7
29	0.12	55	0.42	81	1.2	110	3.2
31	0.14	57	0.45	83	1.3	115	3.7
33	0.15	59	0.49	85	1.4	120	4.3
35	0.17	61	0.54	87	1.5	125	5.0
37	0.18	63	0.58	89	1.6	136	6.6
39	0.20	65	0.63	91	1.7	146	8.7
41	0.22	67	0.68	93	1.8	150	9.9
43	0.24	69	0.74	95	1.9	155	11.
45	0.27	71	0.80	97	2.1	165	14.
47	0.29	73	0.87	99	2.2	175	18.
49	0.32	75	0.93	101	2.4		

Table 5.1.2.5-6, π_T VS. JUNCTION TEMPERATURE FOR HERMETIC LTTL & STTL: NONHERMETIC TTL, HTTL, DTL & ECL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.41	77	1.4	103	3.8
27	0.11	53	0.45	79	1.5	105	4.1
29	0.13	55	0.50	81	1.6	110	4.9
31	0.14	57	0.55	83	1.7	115	5.8
33	0.16	59	0.60	85	1.9	120	6.9
35	0.18	61	0.66	87	2.0	125	8.1
37	0.20	63	0.72	89	2.2	135	11.
39	0.22	65	0.79	91	2.4	145	15.
41	0.24	67	0.87	93	2.6	150	18.
43	0.27	69	0.95	95	2.8	155	20.
45	0.30	71	1.0	97	3.0	165	27.
47	0.33	73	1.1	99	3.3	175	35.
49	0.37	75	1.2	101	3.5		

Table 5.1.2.5-7. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC LSTTL & PMOS; NONHERMETIC LTTL & STTL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.48	77	1.8	103	5.6
27	0.11	53	0.53	79	2.0	105	6.1
29	0.13	55	0.59	81	2.2	110	7.5
31	0.15	57	0.66	83	2.4	115	9.1
33	0.17	59	0.73	85	2.6	120	11.
35	0.19	61	0.81	87	2.9	125	13.
37	0.21	63	0.90	89	3.1	135	19.
39	0.24	65	1.0	91	3.4	145	27.
41	0.27	67	1.1	93	3.7	150	31.
43	0.30	69	1.2	95	4.0	155	37.
45	0.34	71	1.4	97	4.4	165	50.
47	0.38	73	1.5	99	4.8	175	67.
49	0.43	75	1.6	101	5.2		

Table 5.1.2.5-8. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC NMOS & CCD; NONHERMETIC LSTTL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.56	77	2.4	103	8.4
27	0.12	53	0.63	79	2.7	105	9.2
29	0.13	55	0.71	81	3.0	110	12.
31	0.15	57	0.80	83	3.3	115	14.
33	0.18	59	0.89	85	3.6	120	18.
35	0.20	61	1.0	87	4.0	125	22.
37	0.23	63	1.1	89	4.4	135	32.
39	0.26	65	1.3	91	4.8	145	46.
41	0.30	67	1.4	93	5.3	150	56.
43	0.34	69	1.6	95	5.8	155	66.
45	0.38	71	1.8	97	6.4	165	93.
47	0.44	73	1.9	99	7.0	175	129.
49	0.49	75	2.2	101	7.7		

Table 5.1.2.5-9. π_T VS. JUNCTION TEMPERATURE FOR HERMETIC IIL & MNOS.

$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T
25	0.10	51	0.65	77	3.2	103	13.
27	0.12	53	0.74	79	3.6	105	14.
29	0.14	55	0.85	81	4.0	110	18.
31	0.16	57	0.96	83	4.5	115	22.
33	0.18	59	1.1	85	5.0	120	28.
35	0.21	61	1.2	87	5.6	125	35.
37	0.25	63	1.4	89	6.2	135	54.
39	0.29	65	1.6	91	6.9	145	81.
41	0.33	67	1.8	93	7.6	150	99.
43	0.38	69	2.0	95	8.5	155	120.
45	0.43	71	2.3	97	9.4	165	173.
47	0.50	73	2.5	99	10.	175	247.
49	0.57	75	2.9	101	11.		

Table 5.1.2.5-10. π_T VS. JUNCTION TEMPERATURE FOR HERMETIC CMOS, LINEAR & SOS

$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T	$T_J(^\circ C)$	π_T
25	0.10	51	0.76	77	4.3	103	19.
27	0.12	53	0.88	79	4.8	105	21.
29	0.14	55	1.0	81	5.5	110	27.
31	0.17	57	1.2	83	6.1	115	35.
33	0.19	59	1.3	85	6.9	120	45.
35	0.23	61	1.5	87	7.8	125	57.
37	0.27	63	1.7	89	8.7	135	91.
39	0.31	65	2.0	91	9.8	145	142.
41	0.36	67	2.3	93	11.	150	175.
43	0.42	69	2.6	95	12.	155	216.
45	0.49	71	2.9	97	14.	165	323.
47	0.57	73	3.3	99	15.	175	473.
49	0.56	75	3.8	101	17.		

TABLE 5.1.2.5-11. π_T VS. JUNCTION TEMPERATURE
FOR NONHERMETIC PMOS.

$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T
25	0.10	51	0.89	77	5.7	103	28
27	0.12	53	1.0	79	6.5	105	32
29	0.14	55	1.2	81	7.4	110	42
31	0.17	57	1.4	83	8.4	115	55
33	0.20	59	1.6	85	9.6	120	72
35	0.24	61	1.9	87	11.	125	93
37	0.29	63	2.2	89	12.	135	154
39	0.34	65	2.5	91	14.	145	248
41	0.40	67	2.9	93	16.	150	311
43	0.47	69	3.3	95	18.	155	390
45	0.55	71	3.8	97	20.	165	500
47	0.65	73	4.4	99	23.	175	907
49	0.76	75	5.0	101	25.		

table 5.1.2.5-12. π_T VS. JUNCTION TEMPERATURE FOR
NONHERMETIC IIL, MNOS, NMOS & CCD

$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T	$T_J(^{\circ}C)$	π_T
25	0.10	51	1.2	77	10	103	63
27	0.12	53	1.5	79	12	105	72
29	0.15	55	1.7	81	14	110	100
31	0.19	57	2.0	83	16	115	136
33	0.23	59	2.4	85	18	120	184
35	0.28	61	2.9	87	21	125	248
37	0.33	63	3.4	89	25	135	439
39	0.40	65	4.0	91	28	145	756
41	0.49	67	4.7	93	32	150	982
43	0.59	69	5.5	95	37	155	1269
45	0.71	71	6.4	97	43	165	2081
47	0.85	73	7.5	99	49	175	3337
49	1.0	75	8.7	101	56		

TABLE 5.1.2.5-13. π_T VS. JUNCTION TEMPERATURE FOR
NONHERMETIC CMOS, LINEAR & SOS.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	1.7	77	18.	103	142.
27	0.13	53	2.0	79	22.	105	165.
29	0.16	55	2.5	81	25.	110	236.
31	0.20	57	3.0	83	30.	115	335.
33	0.25	59	3.6	85	35.	120	472.
35	0.31	61	4.4	87	42.	125	659.
37	0.39	63	5.2	89	49.	135	1252.
39	0.48	65	6.3	91	57.	145	2308.
41	0.60	67	7.5	93	67.	150	3099.
43	0.73	69	9.0	95	78.	155	4134.
45	0.90	71	11.	97	91.	165	7210.
47	1.1	73	13.	99	106.	175	12,272.
49	1.4	75	15.	101	123.		

TABLE 5.1.2.5-26: C_3, PACKAGE COMPLEXITY FAILURE RATES IN
FAILURES PER 10^6 HOURS

Number of Functional Pins	PACKAGE TYPE *				
	Hermetic DIPs with Solder or Weld Seal, Leadless Chip Carriers (LCC)	Hermetic DIPs with Glass Seal	Nonhermetic DIPs	Hermetic Flatpacks	Hermetic Cans
3	---	---	---	---	---
4	---	---	---	0.0004	0.0005
6	0.0019	0.0013	0.0018	0.0008	0.0011
8	0.0026	0.0021	0.0026	0.0013	0.0020
10	0.0034	0.0029	0.0034	0.0020	0.0031
12	0.0041	0.0038	0.0043	0.0028	0.0044
14	0.0048	0.0048	0.0051	0.0037	0.0060
16	0.0056	0.0059	0.0061	0.0047	0.0079
18	0.0064	0.0071	0.0070	0.0058	---
22	0.008	0.010	0.009	0.008	---
24	0.009	0.011	0.010	0.010	---
28	0.010	0.014	0.012	---	---
36	0.013	0.020	0.016	---	---
40	0.015	0.024	0.019	---	---
64	0.025	0.048	0.033	---	---
80	0.032	---	---	---	---
128	0.053	---	---	---	---

*If seal type for hermetic DIP is unknown, assume glass seal.

The tabulated values are determined by the following equations:

Hermetic DIPs with solder or weld seals, Leadless Chip Carrier (LCC) $\qquad C_3 = 2.8 \times 10^{-4}(N_p)^{1.08}$

Hermetic DIPs with glass seals $\qquad C_3 = 9.0 \times 10^{-5}(N_p)^{1.51}$

Nonhermetic DIPs $\qquad C_3 = 2.0 \times 10^{-4}(N_p)^{1.23}$

Hermetic Flatpacks $\qquad C_3 = 3.0 \times 10^{-5}(N_p)^{1.82}$

Hermetic Cans $\qquad C_3 = 3.0 \times 10^{-5}(N_p)^{2.01}$

where: N_p is the number of pins on a device package which are connected to some substrate location ($3 \leq N_p \leq 128$).

Example Calculation

Consider a Zilog Z80 microprocessor in a 40 pin ceramic package with a metal lid. The device is installed in an Airborne, Uninhabited Trainer environment and is operating at a case temperature of 95°C. The device has been screened to full MIL-M-38510 Class B requirements. It dissipates 0.500 watts and has a case to junction thermal resistance of 40°C/watt. The junction temperature is therefore 95°C + (0.500w)(40°C/watt) = 115°C.

The microcprocessor has been fabricated using NMOS technology. It has 2833 gates and 248 bits (26 8-bit registers, 3 8-bit buffer/registers, 1 16-bit buffer/register).

$$\lambda_p = \pi_Q (0.0615\pi_T + C_3\pi_E) \pi_L$$

From Table 5.1.2.5-1 π_Q = 2.0
From Table 5.1.2.5-2 π_L = 1.0 since the Z80 is a mature part
From Table 5.1.2.5-8 π_T = 14.0
From Table 5.1.2.5-3 π_E = 4.0
From Table 5.1.2.5-26 C_3 = 0.015

Thus

$$\lambda_p = 2.0 \quad (0.0615)(14.0) + (0.015)(4.0) \quad 1.0$$

$$= 1.84 \text{ failures}/10^6 \text{ hours}$$

A-15

Appendix A

Section 2: Proposed Hybrid Microcircuit Failure Rate Prediction Model

5.1.2.7 <u>Hybrid Microcircuit</u>

5.1.2.7.1 <u>Hybrid Prediction Model</u>

$$\lambda_p = \lambda_b\ \pi_E\ \pi_Q\ \pi_T\ \pi_L\ \pi_F \quad \text{(failures/10}^6\text{ hours)}$$

where

λ_b is the base failure rate, as a function of the number of
   interconnects from Table 5.1.2.7-1

π_E is the environmental factor from Table 5.1.2.7-2

π_Q is the quality factor from Table 5.1.2.7-3

π_T is the temperature factor from Table 5.1.2.7-4

π_L is the learning factor from Table 5.1.2.7-5

π_F is the function factor from Table 5.1.2.7-6

Base Failure Rate

The base failure rate λ_b is defined as

$$\lambda_b = 0.17 \ (N_I)^{0.36} \text{ failures per } 10^6 \text{ hours}$$

Interconnections, as defined for this model are counted as one for every wire. Each beam lead or solder bump shall also be counted as one interconnection.

Only active (current carrying) interconnections shall be counted

Active die attach bonds (die to substrate bonds) are not counted as interconnections

Redundant interconnections shall be counted as only one interconnection

If an accurate count of the actual interconnections can not be obtained, the following approximations may be made:

Component	Number of Interconnections
Each IC	(Number of chip bonding pads.)
Each Transistor	2
Each Diode	1
Each Capacitor	2
Each External Lead	1
Each Chip Resistor	2

TABLE 5.1.2.7-1: HYBRID BASE FAILURE RATE

N_I	λ_b	N_I	λ_b
10	.39	240	1.22
20	.50	250	1.24
30	.58	260	1.26
40	.64	270	1.28
50	.70	280	1.29
60	.74	290	1.31
70	.78	300	1.32
80	.82	310	1.34
90	.86	320	1.36
100	.89	330	1.37
110	.92	340	1.39
120	.95	350	1.40
130	.98	360	1.41
140	1.01	370	1.43
150	1.03	380	1.44
160	1.06	390	1.46
170	1.08	400	1.47
180	1.10	410	1.48
190	1.12	420	1.50
200	1.15	430	1.51
210	1.17	440	1.52
220	1.19	450	1.53
230	1.20		

Environmental Factor

TABLE 5.1.2.7-2: ENVIRONMENTAL FACTOR FOR HYBRIDS

Environment	π_E	Environment	π_E
G_B	0.38	A_{IA}	4.0
G_F	2.5	A_{IF}	6.0
G_M	4.2	A_{UC}	3.0
M_P	3.8	A_{UT}	4.0
N_{SB}	4.0	A_{UB}	7.5
N_S	4.0	A_{UA}	6.0
N_U	5.7	A_{UF}	9.0
N_H	5.9	S_F	0.90
N_{UU}	6.3	M_{FF}	3.9
A_{RW}	8.5	M_{FA}	5.4
A_{IC}	2.5	U_{SL}	11.0
A_{IT}	3.0	M_L	13.0
A_{IB}	5.0	C_L	220.

TABLE 5.1.2.7-3: QUALITY FACTORS (π_Q) FOR HYBRIDS

Quality Level	Description	π_Q
S	Procured to the Class S requirements of MIL-STD-883, Method 5008 and Appendix G of MIL-M-38510. or MIL-STD-883, Methods 5004 and 5005 and MIL-M-38510	0.5
B	Procured to the Class B requirements of MIL-STD-883, Method 5008 and Appendix G of MIL-M-38510. or MIL-STD-883, Methods 5004 and 5005 and MIL-M-38510	1.0
D	Commercial Part, hermetically sealed, with no screening beyond manufacturer's normal quality assurance practices	60.0
D-1	Commercial Part, non-hermetically sealed, with no screening beyond manufacturer's normal quality assurance practices	120.0

Temperature Factor

The temperature factor π_T for hybrids is defined as

$$\pi_T = \exp 3708 \left(\frac{1}{298} - \frac{1}{T_C + 273}\right) .$$

T_C = case temperature of the hybrid (°C)

TABLE 5.1.2.7-4: Temperature Factor

T_C	π_T	T_C	π_T
25	1.00	67	4.65
27	1.09	69	4.96
29	1.18	71	5.28
31	1.28	73	5.62
33	1.38	75	5.98
35	1.50	77	6.35
37	1.62	79	6.75
39	1.75	81	7.16
41	1.89	83	7.59
43	2.03	85	8.05
45	2.19	87	8.52
47	2.35	89	9.02
49	2.53	91	9.55
51	2.71	93	10.09
53	2.91	95	10.66
55	3.12	97	11.26
57	3.34	99	11.88
59	3.58	101	12.53
61	3.82	103	13.21
63	4.08	105	13.92
65	4.36	107	14.66
		109	15.43

If T_C cannot be determined, use the following:

ENVIRO.	G_B	S_F	G_F	N_{SB}	N_S	M_P	G_M	M_{FF}	A_{IT}	M_{FA}	A_{IC}	A_{IB}	A_{IA}
T_C (°C.)	35	40	45	45	45	40	50	60	60	50	60	60	60

ENVIRO.	N_U	A_{UT}	N_H	N_{UU}	A_{RW}	A_{IF}	U_{SL}	A_{UF}	M_L	C_L	A_{UF}	A_{UB}	A_{UA}
T_C (°C.)	80	95	45	25	60	60	40	95	60	45	35	95	95

Learning Factor

The learning factor π_L for hybrid is defined as

$$\pi_L = \begin{cases} 84 \ N_p^{-0.67} & \text{custom hybrids with } 50 < N_p < 5000 \\ 0.28 & \text{all off-the-shelf hybrids \& custom hybrids with } N_p \geq 5000 \\ 6.00 & N_p < 50 \end{cases}$$

N_p = total number of hybrid produced (made)

TABLE 5.1.2.7-5: LEARNING FACTOR

N_p	πL	N_p	πL
50	6.11	750	1.00
75	4.66	800	0.95
100	3.84	850	0.92
125	3.31	900	0.88
150	2.93	950	0.85
175	2.64	1000	0.82
200	2.41	1100	0.77
225	2.23	1200	0.73
250	2.08	1300	0.69
275	1.95	1400	0.66
300	1.84	1500	0.63
325	1.74	1600	0.60
350	1.66	1700	0.58
375	1.58	1800	0.55
400	1.52	1900	0.53
425	1.46	2000	0.52
450	1.40	2500	0.44
475	1.35	3000	0.39
500	1.31	3500	0.35
550	1.23	4000	0.32
600	1.16	4500	0.30
650	1.10	5000	0.28
700	1.04		

Function Factor

TABLE 5.1.2.7-6: FUNCTION FACTOR

πF	FUNCTION
0.1	*Passive hybrids
1.0	All other hybrids

* Hybrids with no active element (i.e. resistor networks)

A-23

5.1.2.7-2 Example Calculation

Consider a hybrid to be employed in an Airborne, Inhabited Fighter environment, having an ambient temperature of 55°C and a case temperature 6°C above ambient. Five-hundred and fifty hybrids will be required, including spares. The hybrid contains several active components and has 90 interconnections. These will be screened to Class B specifications.

From Table 5.1.2.7-1, λ_b = 0.86
From Table 5.1.2.7-2, π_E = 6.0
From Table 5.1.2.7-3, π_Q = 1.0
From Table 5.1.2.7-4, π_T = 3.82
From Table 5.1.2.7-5, π_L = 1.23
From Table 5.1.2.7-6, π_F = 1.0

Thus the predicted failure rate λ_p is given by

$$\lambda_p = (1.23)\ (6.0)\ (1.0)\ (3.82)\ (0.86)\ (1.0) = 24.24 \text{ failures}/10^6 \text{ hrs}$$

Appendix A:

Section 3: Proposed Analog Microprocessor
Failure Rate Prediction Model

5.1.2.3 <u>Monolithic Bipolar, MOS Random Logic LSI, Microprocessor and</u>
<u>Analog Microprocessor Devices (equal to or greater than 100</u>
<u>gates)</u>.

Part operating failure rate model (λ_p):

$$\lambda_p = \pi_Q \pi_A \left[C_1 \pi_T \pi_V \pi_{PT} + (C_2 + C_3) \pi_E \right] \pi_L \quad \text{Failures/10}^6 \text{ hours} =$$

where

λ_p is the device failure rate in F/10^6 hours

π_Q is the quality factor, Table 5.1.2.5-1

π_A is the analog signal factor, Table 5.1.2.5-27

π_T is the temperature acceleration factor, based on technology
(Table 5.1.2.5-4) and is found in Tables 5.1.2.5-5 thru 5.1.2.5-13.

π_V is the voltage derating stress factor, Table 5.1.2.5-14

π_{PT} is the ROM and PROM programming technique factor. For
microprocessors containing on-chip ROMs or PROMs, Table 5.1.2.5-
25, otherwise π_{PT} is equal to one

π_E is the application environment factor, Table 5.1.2.5-3

C_1 & C_2 are the circuit complexity failure rates based upon gate count
and are found in Tables 5.1.2.5-20 and 5.1.2.5-21. Analog
microprocessor gate count shall be determined from the digital
portion only. (See Tables 5.1.2.5-27 and 5.1.2.5-28 for gate
count determination)

C_3 is the package complexity failure rate, Table 5.1.2.5-26

π_L is the device learning factor, Table 5.1.2.5-2

MICROELECTRONIC DEVICES
MONOLITHIC

5.1.2.5 Tables for the Monolithic Model Parameters

TABLE 5.1.2.5-1. Π_Q, QUALITY FACTORS

Quality Level	Description	Π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements.	0.5
B	Procured in full accordance with MIL-M-38510, Class B requirements.	1.0
B-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class B, and the qualification requirements of Method 5005, Class B. Generic data may be substituted for Groups C&D.	3.0
B-2	Procured to vendor's equivalent of screening requirements of MIL-STD-883, Method 5004, Class B, and in accordance with vendor's electrical parameters. Vendor waives certain requirements of MIL-STD-883, Method 5004, Class B.	6.5
C	Procured in full accordance with MIL-M-38510, Class C requirements.	8.0
C-1	Procured to screening requirements of MIL-STD-883, Method 5004, Class C, and the qualification requirements of Method 5005. Class C. Generic data may be substituted for Groups C&D.	13.0
D	Hermetically sealed part with no screening beyond the manufacturer's regular quality assurance practices; parts encapsulated with organic material.*	17.5
D-1	Commercial (or non-mil standard) part, encapsulated or sealed with organic materials (e.g., epoxy, silicone or phenolic).	35.0

*All encapsulated devices must be subjected to 160 hr. burn-in at 125°C.,10 temperature cycles (-55°C to 125°C.) with end point electricals, and high temperature continuity test at 100°C.

TABLE 5.1.2.5-2. Π_L, LEARNING FACTORS

The learning factor Π_L is 10 under any of the following conditions:

(1) New device in initial production.
(2) Where major changes in design or process have occurred.
(3) Where there has been an extended interruption in production or a change in line personnel (radical expansion).
(4) For all CMOS/SOS devices.

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as six months of continuous production.

Π_L is equal to 1.0 under all production conditions not stated in (1), (2) and (3) above.

TABLE 5.1.2.5-3. APPLICATION ENVIRONMENT FACTOR Π_E

ENVIRONMENT	π_E	ENVIRONMENT	π_E
S_F	0.90	N_U	5.7
G_{MS}	.65		
G_B	0.38	A_{UT}	4.0
G_F	2.5	N_H	5.9
N_{SB}	4.5	N_{UU}	6.3
N_S	3.4	A_{RW}	8.5
M_P	3.8	A_{IF}	7.0
G_M	4.2	U_{SL}	11.
M_{FF}	3.9	A_{UF}	8.0
A_{IT}	3.5	M_L	13.
M_{FA}	5.4	C_L	220.

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-4. TECHNOLOGY TEMPERATURE FACTOR TABLES
(SEE NOTES BELOW)

Technology	Package Type	Π_T Table Number	A
TTL, HTTL, DTL & ECL	Hermetic Nonhermetic	5.1.2.5-5 5.1.2.5-6	4635. 5214.
LTTL & STTL	Hermetic Nonhermetic	5.1.2.5-6 5.1.2.5-7	5214. 5794.
LSTTL	Hermetic Nonhermetic	5.1.2.5-7 5.1.2.5-8	5794. 6373.
IIL & MNOS	Hermetic Nonhermetic	5.1.2.5-9 5.1.2.5-12	6952. 9270.
PMOS	Hermetic Nonhermetic	5.1.2.5-7 5.1.2.5-11	5794. 8111.
NMOS & CCD	Hermetic Nonhermetic	5.1.2.5-8 5.1.2.5-12	6373. 9270.
CMOS, CMOS/SOS & Linear	Hermetic Nonhermetic	5.1.2.5-10 5.1.2.5-13	7532. 10429.

Note 1. $\Pi_T = 0.1e^x$

where $x = -A \left(\dfrac{1}{T_J + 273} - \dfrac{1}{298} \right)$

A = value from above Table

T_J = device worst case junction temperature ($^\circ$C).

e = natural logarithm base, 2.718

A-29

(Notes continued for Table 5.1.2.5-4

NOTE 2. T_J, the worst case junction temperature, shall be estimated
using the following expression:

$$T_J = T_C + \theta_{JC} \, P$$

where: T_C is case temperature (°C.).

θ_{JC} is junction to case thermal resistance (°C/watt) for a device
soldered into a printed circuit board. If θ_{JC} is not available,
use a value contained in a specification for the closest equivalent
device or use the table below.

P is the worst case power realized in a system application. If the
applied power is not available, use the maximum power dissipation
from the device specification or from the specification for the
closest equivalent device.

If T_C cannot be determined, use the following:

ENVIRO.	G_B	S_F	G_F	N_{SB}	N_S	M_P	G_M	M_{FF}	A_{IT}	M_{FA}	A_{IC}	A_{IA}	A_{IS}
T_C (°C.)	35	40	45	45	45	40	50	60	60	50	60	60	60

ENVIRO.	N_U	A_{UT}	N_H	N_{UU}	A_{RW}	A_{IF}	U_{SL}	A_{UF}	M_L	C_L	A_{UC}	A_{UA}	A_{UB}
T_C (°C.)	80	95	45	25	60	60	40	95	60	45	95	95	95

If θ_{JC} cannot be determined, use the following:

Package Type	Die Attach*	Number of Package Pins	
		$\leq$ 22 pins	> 22 pins
Leadless Chip Car-riers (LCCs) Hermetic DIPs	Eutectic Epoxy or Glass	30 125	25 100
Nonhermetic DIPs	Eutectic Epoxy or Glass	30 125	25 100
Hermetic Flatpacks	Eutectic Epoxy or Glass	40 125	35 100
Hermetic Cans	Eutectic Epoxy or Glass	30 125	NA NA

* If the die attach method cannot be determined, assume that epoxy die attach is
used for hermetically packaged CMOS and eutectic die attach for all other her-
metic packages.

MICROELECTRONIC DEVICES
MONOLITHIC

Table 5.1.2.5-5. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC TTL, HTTL, DTL, & ECL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.35	77	1.0	103	2.5
27	0.11	53	0.38	79	1.1	105	2.7
29	0.12	55	0.42	81	1.2	110	3.2
31	0.14	57	0.45	83	1.3	115	3.7
33	0.15	59	0.49	85	1.4	120	4.3
35	0.17	61	0.54	87	1.5	125	5.0
37	0.18	63	0.58	89	1.6	136	6.6
39	0.20	65	0.63	91	1.7	146	8.7
41	0.22	67	0.68	93	1.8	150	9.9
43	0.24	69	0.74	95	1.9	155	11.
45	0.27	71	0.80	97	2.1	165	14.
47	0.29	73	0.87	99	2.2	175	18.
49	0.32	75	0.93	101	2.4		

Table 5.1.2.5-6, π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC LTTL & STTL: NONHERMETIC TTL, HTTL, DTL & ECL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.41	77	1.4	103	3.8
27	0.11	53	0.45	79	1.5	105	4.1
29	0.13	55	0.50	81	1.6	110	4.9
31	0.14	57	0.55	83	1.7	115	5.8
33	0.16	59	0.60	85	1.9	120	6.9
35	0.13	61	0.66	87	2.0	125	8.1
37	0.20	63	0.72	89	2.2	135	11.
39	0.22	65	0.79	91	2.4	145	15.
41	0.24	67	0.87	93	2.6	150	18.
43	0.27	69	0.95	95	2.8	155	20.
45	0.30	71	1.0	97	3.0	165	27.
47	0.33	73	1.1	99	3.3	175	35.
49	0.37	75	1.2	101	3.5		

MICROELECTRONIC DEVICES
MONOLITHIC

Table 5.1.2.5-7. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC LSTTL & PMOS; NONHERMETIC LTTL & STTL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.48	77	1.8	103	5.6
27	0.11	53	0.53	79	2.0	105	6.1
29	0.13	55	0.59	81	2.2	110	7.5
31	0.15	57	0.66	83	2.4	115	9.1
33	0.17	59	0.73	85	2.6	120	11.
35	0.19	61	0.81	87	2.9	125	13.
37	0.21	63	0.90	89	3.1	135	19.
39	0.24	65	1.0	91	3.4	145	27.
41	0.27	67	1.1	93	3.7	150	31.
43	0.30	69	1.2	95	4.0	155	37.
45	0.34	71	1.4	97	4.4	165	50.
47	0.38	73	1.5	99	4.8	175	67.
49	0.43	75	1.6	101	5.2		

Table 5.1.2.5-8. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC NMOS & CCD; NONHERMETIC LSTTL.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.56	77	2.4	103	8.4
27	0.12	53	0.63	79	2.7	105	9.2
29	0.13	55	0.71	81	3.0	110	12.
31	0.15	57	0.80	83	3.3	115	14.
33	0.18	59	0.89	85	3.6	120	18.
35	0.20	61	1.0	87	4.0	125	22.
37	0.23	63	1.1	89	4.4	135	32.
39	0.26	65	1.3	91	4.8	145	46.
41	0.30	67	1.4	93	5.3	150	56.
43	0.34	69	1.6	95	5.8	155	66.
45	0.38	71	1.8	97	6.4	165	93.
47	0.44	73	1.9	99	7.0	175	129.
49	0.49	75	2.2	101	7.7		

MICROELECTRONIC DEVICES
MONOLITHIC

Table 5.1.2.5-9. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC IIL & MNOS.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.65	77	3.2	103	13.
27	0.12	53	0.74	79	3.6	105	14.
29	0.14	55	0.85	81	4.0	110	18.
31	0.16	57	0.96	83	4.5	115	22.
33	0.18	59	1.1	85	5.0	120	28.
35	0.21	61	1.2	87	5.6	125	35.
37	0.25	63	1.4	89	6.2	135	54.
39	0.29	65	1.6	91	6.9	145	81.
41	0.33	67	1.8	93	7.6	150	99.
43	0.38	69	2.0	95	8.5	155	120.
45	0.43	71	2.3	97	9.4	165	173.
47	0.50	73	2.5	99	10.	175	247.
49	0.57	75	2.9	101	11.		

Table 5.1.2.5-10. π_T VS. JUNCTION TEMPERATURE FOR
HERMETIC CMOS, LINEAR & SOS

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.76	77	4.3	103	19.
27	0.12	53	0.88	79	4.8	105	21.
29	0.14	55	1.0	81	5.5	110	27.
31	0.17	57	1.2	83	6.1	115	35.
33	0.19	59	1.3	85	6.9	120	45.
35	0.23	61	1.5	87	7.8	125	57.
37	0.27	63	1.7	89	8.7	135	91.
39	0.31	65	2.0	91	9.8	145	142.
41	0.36	67	2.3	93	11.	150	175.
43	0.42	69	2.6	95	12.	155	216.
45	0.49	71	2.9	97	14.	165	323.
47	0.57	73	3.3	99	15.	175	473.
49	0.66	75	3.8	101	17.		

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-11. π_T VS. JUNCTION TEMPERATURE
FOR NONHERMETIC PMOS.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	0.89	77	5.7	103	28
27	0.12	53	1.0	79	6.5	105	32
29	0.14	55	1.2	81	7.4	110	42
31	0.17	57	1.4	83	8.4	115	55
33	0.20	59	1.6	85	9.6	120	72
35	0.24	61	1.9	87	11.	125	93
37	0.29	63	2.2	89	12.	135	154
39	0.34	65	2.5	91	14.	145	248
41	0.40	67	2.9	93	16.	150	311
43	0.47	69	3.3	95	18.	155	390
45	0.55	71	3.8	97	20.	165	600
47	0.65	73	4.4	99	23.	175	907
49	0.76	75	5.0	101	25.		

table 5.1.2.5-12. π_T VS. JUNCTION TEMPERATURE FOR
NONHERMETIC IIL, MNOS, NMOS & CCD

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	1.2	77	10	103	63
27	0.12	53	1.5	79	12	105	72
29	0.15	55	1.7	81	14	110	100
31	0.19	57	2.0	83	16	115	136
33	0.23	59	2.4	85	18	120	184
35	0.28	61	2.9	87	21	125	248
37	0.33	63	3.4	89	25	135	439
39	0.40	65	4.0	91	28	145	756
41	0.49	67	4.7	93	32	150	982
43	0.59	69	5.5	95	37	155	1269
45	0.71	71	6.4	97	43	165	2081
47	0.85	73	7.5	99	49	175	3337
49	1.0	75	8.7	101	56		

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-13. π_T VS. JUNCTION TEMPERATURE FOR
NONHERMETIC CMOS, LINEAR & SOS.

$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T	$T_J(^oC)$	π_T
25	0.10	51	1.7	77	18.	103	142.
27	0.13	53	2.0	79	22.	105	165.
29	0.16	55	2.5	81	25.	110	236.
31	0.20	57	3.0	83	30.	115	335.
33	0.25	59	3.6	85	35.	120	472.
35	0.31	61	4.4	87	42.	125	659.
37	0.39	63	5.2	89	49.	135	1252.
39	0.48	65	6.3	91	57.	145	2308.
41	0.60	67	7.5	93	67.	150	3099.
43	0.73	69	9.0	95	78.	155	4134.
45	0.90	71	11.	97	91.	165	7210.
47	1.1	73	13.	99	106.	175	12,272.
49	1.4	75	15.	101	123.		

TABLE 5.1.2.5-14. π_V, VOLTAGE DERATING STRESS FACTOR

Technology	π_V
CMOS, V_{DD} = 5 volts	1.0
CMOS, 12 volts $\leq V_{DD} \leq$ 15.5 volts	Equation 1 (below) or Table 2.1.5-15.
CMOS, 18 volts $\leq V_{DD} \leq$ 20 volts	Equation 2 (below) or Table 2.1.5-16.
All technologies other than CMOS	1.0

V_{DD} is the maximum recommended operating supply voltage

Equation 1: For maximum recommended operating supply voltage between 12 and 15.5 volts.

$$\pi_V = 0.110 \ e^X$$

where:

$$X = \frac{0.168 \ V_s \ (T_J + 273)}{298}$$

Equation 2: For maximum recommended operating supply voltage between 18 and 20 volts

$$\pi_V = 0.068 \ e^X$$

where:

$$X = \frac{0.135 \ V_s \ (T_J + 273)}{298}$$

V_s is the operating supply voltage in actual application

T_J is the device worst case junction temperature (^oC)

e is the natural logarithm base, 2.718

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-15. Π_V FOR CMOS WITH $12 \leq V_{DD} \leq 15.5$ VOLTS

V_S (V.)	T_J (°C.)						
	25	50	75	100	125	150	175
3	.18	.19	.20	.21	.22	.22	.23
4	.22	.23	.24	.26	.27	.29	.30
5	.25	.27	.29	.31	.34	.36	.39
6	.30	.33	.36	.39	.42	.46	.50
7	.36	.39	.43	.48	.53	.58	.64
8	.42	.47	.53	.59	.66	.74	.83
9	.50	.57	.64	.72	.83	.94	1.1
10	.59	.68	.78	.90	1.0	1.2	1.4
11	.70	.82	.95	1.1	1.3	1.5	1.8
12	.83	.98	1.2	1.4	1.6	1.9	2.3
13	.98	1.2	1.4	1.7	2.0	2.4	2.9
14	1.2	1.4	1.7	2.1	2.5	3.1	3.8
15	1.4	1.7	2.1	2.6	3.2	3.9	4.9

TABLE 5.1.2.5-16. Π_V FOR CMOS WITH $18 \leq V_{DD} \leq 20$ VOLTS.

V_S	T_J (°C.)						
(V.)	25	50	75	100	125	150	175
3	.10	.11	.11	.11	.12	.12	.13
4	.12	.12	.13	.13	.14	.15	.15
5	.13	.14	.15	.16	.17	.18	.19
6	.15	.16	.18	.19	.20	.21	.23
7	.17	.19	.21	.22	.24	.26	.28
8	.20	.22	.24	.26	.29	.31	.34
9	.23	.25	.28	.31	.34	.38	.42
10	.26	.29	.33	.37	.41	.46	.52
11	.30	.34	.39	.44	.49	.56	.63
12	.34	.39	.45	.52	.59	.68	.78
13	.39	.46	.53	.61	.71	.82	.95
14	.45	.53	.62	.72	.85	.99	1.2
15	.51	.61	.72	.86	1.0	1.2	1.4
16	.59	.71	.85	1.0	1.2	1.5	1.7
17	.67	.82	.99	1.2	1.5	1.8	2.1
18	.77	.95	1.2	1.4	1.7	2.1	2.6
19	.88	1.1	1.4	1.7	2.1	2.6	3.2
20	1.0	1.3	1.6	2.0	2.5	3.1	3.9

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-17. C_1 and C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR
BIPOLAR SSI/MSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
1	0.0007	0.0002	22	0.0056	0.0007	44	0.0089	0.0009
2	0.0012	0.0003	24	0.0060	0.0007	46	0.0091	0.0009
4	0.0019	0.0004	26	0.0063	0.0007	48	0.0094	0.0009
6	0.0024	0.0004	28	0.0066	0.0007	50	0.0097	0.0009
8	0.0029	0.0005	30	0.0069	0.0008	55	0.0103	0.0009
10	0.0034	0.0005	32	0.0072	0.0008	60	0.0109	0.0010
12	0.0038	0.0005	34	0.0075	0.0008	65	0.0115	0.0010
14	0.0042	0.0006	36	0.0078	0.0008	70	0.012	0.0010
16	0.0046	0.0006	38	0.0081	0.0008	80	0.013	0.0011
18	0.0050	0.0006	40	0.0083	0.0008	90	0.014	0.0011
20	0.0053	0.0007	42	0.0086	0.0009	99	0.015	0.0012

Tabulated values are derived from the following equations:

$$C_1 = 7.48 \times 10^{-4} (N_G)^{0.654}$$

$$C_2 = 2.19 \times 10^{-4} (N_G)^{0.364}$$

where N_G is the number of gates.

TABLE 5.1.2.5-18. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR MOS
SSI/MSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
1	0.0022	0.0003	22	0.0065	0.0005	44	0.0084	0.0006
2	0.0028	0.0004	24	0.0067	0.0005	46	0.0085	0.0006
4	0.0036	0.0004	26	0.0069	0.0006	48	0.0086	0.0006
6	0.0041	0.0004	28	0.0071	0.0006	50	0.0088	0.0006
8	0.0046	0.0005	30	0.0073	0.0006	55	0.0091	0.0006
10	0.0049	0.0005	32	0.0075	0.0006	60	0.0094	0.0006
12	0.0053	0.0005	34	0.0076	0.0006	65	0.0096	0.0007
14	0.0056	0.0005	36	0.0078	0.0006	70	0.010	0.0007
16	0.0058	0.0005	38	0.0080	0.0006	80	0.010	0.0007
18	0.0061	0.0005	40	0.0081	0.0006	90	0.011	0.0007
20	0.0063	0.0005	42	0.0082	0.0006	99	0.011	0.0007

Tabulated values are derived from the following equations:

$$C_1 = 2.17 \times 10^{-3} (N_G)^{0.357}$$

$$C_2 = 3.11 \times 10^{-4} (N_G)^{0.178}$$

where N_G is the number of gates.

MICROCIRCUIT DEVICES
MONOLITHIC

TABLE 5.1.2.5-19. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR LINEAR DEVICES IN FAILURES PER 10^6 HOURS

No. Trans.	C_1	C_2	No. Trans.	C_1	C_2	No. Trans.	C_1	C_2
4	0.0046	0.0017	64	0.040	0.0074	148	0.077	0.0116
8	0.0079	0.0024	68	0.042	0.0076	156	0.081	0.0119
12	0.011	0.0030	72	0.044	0.0079	164	0.084	0.0122
16	0.014	0.0035	76	0.046	0.0081	172	0.087	0.0126
20	0.016	0.0040	80	0.048	0.0083	180	0.090	0.0129
24	0.019	0.0044	84	0.050	0.0086	188	0.093	0.0132
28	0.021	0.0048	88	0.052	0.0088	196	0.096	0.0135
32	0.023	0.0051	92	0.053	0.0090	204	0.099	0.0138
36	0.026	0.0054	96	0.055	0.0092	220	0.105	0.0143
40	0.028	0.0058	100	0.057	0.0094	236	0.111	0.0149
44	0.030	0.0061	108	0.061	0.0098	252	0.117	0.0154
48	0.032	0.0063	116	0.064	0.0102	268	0.123	0.0159
52	0.034	0.0066	124	0.067	0.0105	284	0.129	0.0164
56	0.036	0.0069	132	0.071	0.0109	300	0.134	0.0169
60	0.038	0.0072	140	0.074	0.0113			

The tabulated values are derived from the following equations:

$$C_1 = 1.57 \times 10^{-3} (N_T)^{0.780}$$

$$C_2 = 8.0 \times 10^{-4} (N_T)^{0.535}$$

where N_T is the number of transistors

TABLE 5.1.2.5-20. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR BIPOLAR
RANDOM LOGIC LSI DEVICES IN FAILURES PER 10^6 HOURS

No. Gates	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
100	0.015	0.0012	850	0.045	0.0021	3400	0.091	0.0031
150	0.019	0.0013	900	0.046	0.0021	3600	0.093	0.0031
200	0.022	0.0014	950	0.048	0.0022	3800	0.096	0.0032
250	0.024	0.0015	1000	0.049	0.0022	4000	0.098	0.0032
300	0.027	0.0016	1200	0.053	0.0023	4250	0.101	0.0033
350	0.029	0.0016	1400	0.058	0.0024	4500	0.104	0.0033
400	0.031	0.0017	1600	0.062	0.0025	4750	0.107	0.0034
450	0.033	0.0018	1800	0.066	0.0026	5000	0.110	0.0034
500	0.034	0.0018	2000	0.069	0.0027	5500	0.116	0.0035
550	0.036	0.0019	2200	0.073	0.0027	6000	0.121	0.0036
600	0.038	0.0019	2400	0.076	0.0028	6500	0.126	0.0037
650	0.039	0.0019	2600	0.079	0.0029	7000	0.131	0.0038
700	0.041	0.0020	2800	0.082	0.0029	7500	0.135	0.0039
750	0.042	0.0020	3000	0.085	0.0030			
800	0.044	0.0021	3200	0.088	0.0030			

Tabulated values are determined by the following equations:

$$C_1 = 1.48 \times 10^{-3} (N_G)^{0.506} \text{ for } N_G \leq 20000$$

$$C_2 = 3.20 \times 10^{-4} (N_G)^{0.279} \text{ for } N_G \leq 20000$$

where N_G is the number of gates.

MIL-HDBK-217D

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-21. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR MOS
RANDOM LOGIC LSI DEVICES IN FAILURES PER 10^6 HOURS

No. GATES	C_1	C_2	No. Gates	C_1	C_2	No. Gates	C_1	C_2
100	0.011	0.0007	850	0.026	0.0012	3400	0.045	0.0016
150	0.013	0.0008	900	0.027	0.0012	3600	0.046	0.0016
200	0.015	0.0008	950	0.027	0.0012	3800	0.047	0.0016
250	0.016	0.0009	1000	0.028	0.0012	4000	0.048	0.0016
300	0.017	0.0009	1200	0.030	0.0013	4250	0.049	0.0017
350	0.018	0.0009	1400	0.032	0.0013	4500	0.051	0.0017
400	0.019	0.0010	1600	0.033	0.0013	4750	0.052	0.0017
450	0.020	0.0010	1800	0.035	0.0014	5000	0.053	0.0017
500	0.021	0.0010	2000	0.037	0.0014	5500	0.055	0.0018
550	0.022	0.0010	2200	0.038	0.0014	6000	0.057	0.0018
600	0.023	0.0011	2400	0.039	0.0015	6500	0.059	0.0018
650	0.023	0.0011	2600	0.041	0.0015	7000	0.060	0.0019
700	0.024	0.0011	2800	0.042	0.0015	7500	0.062	0.0019
750	0.025	0.0011	3000	0.043	0.0015			
800	0.025	0.0011	3200	0.044	0.0016			

Tabulated values are determined by the following equations:

$$C_1 = 1.75 \times 10^{-3} (N_G)^{0.400} \text{ for } N_G \leq 20000$$

$$C_2 = 2.52 \times 10^{-4} (N_G)^{0.226} \text{ for } N_G \leq 20000$$

where N_G is the number of gates.

Note: This table applies to both static and dynamic operation devices.

A-43

TABLE 5.1.2.5-22. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR
BIPOLAR RAMs IN FAILURES PER 10^6 HOURS

No. Bits	C_1	C_2
16	0.011	0.0002
32	0.016	0.0003
64	0.024	0.0004
128	0.036	0.0006
256	0.054	0.0009
320	0.061	0.0010
512	0.080	0.0013
576	0.086	0.0014
1024	0.119	0.0019
2048	0.178	0.0027
2560	0.202	0.0031
4096	0.265	0.0040
8192	0.395	0.0059
9216	0.423	0.0063
16,384	0.589	0.0086

Tabulated values are determined by the following equations:

$$C_1 = 2.2 \times 10^{-3} (B)^{0.576}$$
$$C_2 = 4.0 \times 10^{-5} (B)^{0.554}$$

where B is the number of bits ($\leq$ 16,384)

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-23. C_1 AND C_2, CIRCUIT COMPLEXITY FAILURE RATES FOR CCDS & MOS RAMs IN FAILURES PER 10^6 HOURS

No. Bits	MOS DYNAMIC & CCD		STATIC	
	C_1	C_2	C_1	C_2
16	0.003	0.00015	0.004	0.00022
32	0.004	0.00023	0.006	0.00033
64	0.006	0.00034	0.009	0.0005
128	0.010	0.0005	0.014	0.0008
256	0.015	0.0008	0.022	0.0012
320	0.017	0.0009	0.026	0.0013
512	0.022	0.0012	0.035	0.0018
1024	0.034	0.0017	0.055	0.0027
2048	0.052	0.0026	0.087	0.0042
2560	0.060	0.0030	0.101	0.0048
4096	0.080	0.0039	0.137	0.0063
8192	0.122	0.0058	0.216	0.0097
9216	0.131	0.0063	0.233	0.0104
16,384	0.186	0.0088	0.339	0.015
32,768	0.284	0.013	0.533	0.022
65,536	0.434	0.020	0.838	0.034

Tabulated values are determined by the following equations:

Dynamic RAMs $\quad C_1 = 5.0 \times 10^{-4} (B)^{0.610}, \quad C_2 = 3.0 \times 10^{-5} (B)^{0.585}$

Static RAMs $\quad C_1 = 6.0 \times 10^{-4} (B)^{0.653}, \quad C_2 = 4.0 \times 10^{-5} (B)^{0.609}$

where B is the number of bits ($\leq 65,536$)

TABLE 5.1.2.5.-24. C_1 AND C_2, DEVICE COMPLEXITY FAILURE RATES FOR ROMs
AND PROMs IN FAILURES PER 10^6 HOURS

No. Bits	Bipolar		MOS	
	C_1	C_2	C_1	C_2
16	0.0026	0.00013	0.0039	0.00020
32	0.0034	0.00017	0.0052	0.00026
64	0.0044	0.00022	0.0070	0.00035
128	0.0058	0.00028	0.0094	0.00046
256	0.0076	0.00037	0.013	0.00060
320	0.0083	0.0004	0.014	0.00066
512	0.010	0.0005	0.017	0.0008
1024	0.013	0.0006	0.023	0.0010
2048	0.017	0.0008	0.031	0.0014
2560	0.018	0.0009	0.034	0.0015
4096	0.022	0.0010	0.041	0.0018
8192	0.029	0.0014	0.055	0.0024
9216	0.030	0.0014	0.058	0.0025
16,384	0.038	0.0018	0.074	0.0032
32,768	0.050	0.0023	0.100	0.0042
65,536	0.065	0.0030	0.134	0.0055

Tabulated values are determined from the following equations:

Bipolar $C_1 = 8.8 \times 10^{-4}(B)^{0.388}$, $C_2 = 4.5 \times 10^{-5}(B)^{0.378}$

MOS $C_1 = 1.2 \times 10^{-3}(B)^{0.425}$, $C_2 = 6.6 \times 10^{-5}(B)^{0.399}$

where B is the number of bits ($\leq 65,536$)

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-25. π_{PT}, ROM AND PROM PROGRAMMING TECHNIQUE FACTORS

Device Type	Technology	Programming Technique	π_{PT}
ROM	Bipolar	Metal Mask	1.0
	MOS	Metal Mask	1.0
PROM	Bipolar	NiCr or TiW Links	*
		Polysilicon Links	*
		Shorted Junction (AIM)	*
	MOS	UV and Electrically Erasable	**

* - For Bipolar PROMs utilizing NiCr, TiW, Polysilicon or
Shorted Junction (AIM) Links:
$$\pi_{PT} = 0.985 + 9.5 \times 10^{-5}(B)$$

where B is the number of bits.

** - For MOS PROMs, both UV and Electrically Erasable:

$$\pi_{PT} = 0.950 + 7.5 \times 10^{-5}(B)$$

where B is the number of bits.

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-26. C_3, PACKAGE COMPLEXITY FAILURE RATES IN FAILURES
PER 10^6 HOURS

Number of Functional Pins	PACKAGE TYPE *				
	Hermetic DIPs with Solder or Weld Seal	Hermetic DIPs with Glass Seal	Nonhermetic DIPS	Hermetic Flatpacks	Hermetic Cans
3	---	---	---	---	0.0003
4	---	---	---	0.0004	0.0005
6	0.0019	0.0013	0.0018	0.0008	0.0011
8	0.0026	0.0021	0.0026	0.0013	0.0020
10	0.0034	0.0029	0.0034	0.0020	0.0031
12	0.0041	0.0038	0.0043	0.0028	0.0044
14	0.0048	0.0048	0.0051	0.0037	0.0060
16	0.0056	0.0059	0.0061	0.0047	0.0079
18	0.0064	0.0071	0.0070	0.0058	---
22	0.008	0.010	0.009	0.008	---
24	0.009	0.011	0.010	0.010	---
28	0.010	0.014	0.012	---	---
36	0.013	0.020	0.016	---	---
40	0.015	0.024	0.019	---	---
64	0.025	0.048	0.033	---	---

*If seal type for hermetic DIP is unknown, assume glass seal.

The tabulated values are determined by the following equations:

Hermetic DIPs with solder or weld seals $\quad C_3 = 2.8 \times 10^{-4}(N_p)^{1.08}$

Hermetic DIPs with glass seals $\quad C_3 = 9.0 \times 10^{-5}(N_p)^{1.51}$

Nonhermetic DIPs $\quad C_3 = 2.0 \times 10^{-4}(N_p)^{1.23}$

Hermetic Flatpacks $\quad C_3 = 3.0 \times 10^{-5}(N_p)^{1.82}$

Hermetic Cans $\quad C_3 = 3.0 \times 10^{-5}(N_p)^{2.01}$

where: N_p is the number of pins on a device package which are connected to some substrate location.

MICROELECTRONIC DEVICES
MONOLITHIC

TABLE 5.1.2.5-27: π_A, ANALOG SIGNAL FACTOR

Device Type	π_A
Monolithic Bipolar	1.0
MOS Random Logic LSI	1.0
Microprocessor	1.0
Analog Microprocessor*	1.24

* Analog microprocessor is defined as any microprocessor with on-chip
circuitry capable of accepting or outputting an analog signal.

Appendix B

References

B-1

References:

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2. Barbe, D.F., "Very Large Scale Integrated Circuits, Fundamentals and Applications" Second Edition, Springer 1982.

3. Grubin, H.L., and Ferry, D.K., "Conceptual Problems in Modeling Submicron Device Physics" Journal of Vacuum Science Technology 19(3) September/October 1981.

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19. Crook and Meyer, Redundancy Reliability, 1981 Proceedings, International Reliability Physics Symposium, pp 1-10.

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23. Mead, C. and L. Conway, Introduction to VLSI Systems Addison-Wesley, 1979.

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26. Valdya, S., Fraser, D.B. and Sinha, A.K. (Bell Labs., Murray Hill, NJ) ELECTROMIGRATION RESISTANCE OF FINE-LINE Al FOR VLSI APPLICATIONS. pp 165-170. Cat. no. 80CH1531-3.

Appendix C

Vendors Contacted for Reliability Data

Phase 1: VLSI and Hybrid Microcircuits

END

FILMED

DTIC

1.0 4.5 2.8 2.5
5.0
5.6 3.2 2.2
6.3
3.6
7.1
1.1 4.0 2.0

1.8

1.25 1.4 1.6

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A
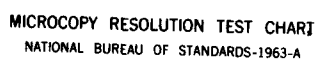
1. Unitrode Corporation
   Lexington, MA
   Negative Reply

2. Circuit Technology
   Farmingdale, NY
   Sent Hybrid Data

3. Monolithic Memories
   Sunnyvale, CA
   Sent Data

4. Nitron
   Cupertino, CA
   Sent Data

5. Codex Corporation
   Mansfield, MA
   No Response

6. Silicon General
   Garden Grove, CA
   No Response

7. Synertec
   Santa Clara, CA
   Sent Data

8. Siliconix
   Santa Clara, CA
   Negative Reply

9. Advanced Micro Devices
   Sunnyvale, CA
   Sent Data

10. Interdesign
    Sunnyvale, CA
    Sent Data

11. Varian Associates
    Palo Alto, CA
    No Response

12. American Microsystems, Inc.
    Santa Clara, CA
    No Response

13. Intel
    Santa Clara, CA
    Sent Data

14. National Semiconductor
    Santa Clara, CA
    Sent Data

15. Signetics
    Sunnyvale, CA
    Promised Data

16. Fairchild
    Mt. View, CA
    Sent Data

17. NCR Microelectronics
    Miamisburg, OH
    No Response

18.	Hughes Aircraft Irvine, CA	No Response
19.	RCA Solid State Sommerville, NJ	Will Not Send Data
20.	Harris Semiconductor Melbourne, FL	No Response
21.	Burr-Brown Tucson, AZ	Promised Data
22.	Exxar-Integrated Systems Sunnyvale, CA	No Response
23.	Precision Monolithics Santa Clara, CA	No Response
24.	Collins Communication Systems Richardson, TX	No Response
25.	Zilog Cupertino, CA	Sent Updates
26.	Mostek Carrolton, TX	Sent Data
27.	Intersil Cupertino, CA	Sent Data
28.	Texas Instruments Dallas, TX	No Response
29.	Texas Instruments Houston, TX	No Response
30.	Motorola Mesa, AZ	No Response
31.	Teledyne Semiconductor Mt. View, CA	No Response
32.	Micro Networks Worcester, MA	Promised Data
33.	Solid State Scientific Montgomeryville, PA	No Response

34.	TRW Redondo Beach, CA	Negative Replay No Data Available
35.	TRW Torrance, CA	Sent Data
36.	United Technologies Microelectronics Colorado Springs, CO	No Response
37.	Analog Devices Semiconductor Wilmington, MA	No Data Available
38.	Analog Devices, Inc. Norwood, MA	Sent Data
39.	Beckman Instruments Fullerton, CA	No Response
40.	General Instrument Corporation Hicksville, NY	No Response
41.	IIT Semiconductors Lawarence, MA	No Response
42.	3M St. Paul, MN	No Response
44.	Optical Electronics Tucson, AZ	No Response
45.	OKI Electronics Ft. Lauderdale, Fl	No Response
46.	Sprague Electric Worcester, MA	Received Data
47.	Western Electric	Negative Reply
48.	Motorola Austin, TX	Received Data
49.	Hitachi America, LTD San Jose, CA	No Response
50.	Silicon General Garden Grove, CA	No Response
51.	Honeywell Plymouth, MN	Promised Data

52.	Zenith Glenview, IL	Promised Data
53.	Magnavox Torrance, CA	Promised Data
54.	Raytheon Quincy, MA	Promised Hybrid Data
55.	California Devices San Jose, CA	Promised Data
56.	Micro-Pac Industries Garland TX	Promised Data
57.	Teleydyne Philbrick Dedham, MA	No Data Available
58.	Micro Networks Worcester, MA	Promised Data
59.	Raytheon Mt. View, CA	Promised Data
60.	Hughes Aircraft Fullerton, CA	Sent Data
61.	Data General Westboro, MA	Promised Data
62.	Ventronics, INc. Kenilworth, NJ	No Response
63.	Aeroflex Labs, Inc. Plainview, NY	No Response
64.	Alpha Industries, INc. Woburn, MA	No Response
65.	American Electronics Labs Lansdale, PA	No Response
66.	Avantek, Inc. Santa Clara, CA	No Response
67.	Aydin Vector Division Newton, PA	No Response
68.	Ball Corporation Huntington Beach, CA	No Response

69.	BBN Instrument Corporation Fullerton, CA	No Response
70.	CTS Microelectronics West Lafayette, IN	No Response
71.	Datel Intersil Mansfield, MA	Received Data
72.	Film Microelectronics Burlington, MA	No Response
73.	HEI Chaska, MN	No Response
74.	Hybrid Systems Billerica, MA	Received Data
75.	Hytek Microsystems Los Gatos, CA	No Response
76.	ILC Data Device Corporation Bohemia, NY	Negative Reply
77.	Intech Inc. Santa Clara, CA	No Response
78.	Integrated Circuits Bellevue, WA	Will not send data (Proprietary)
79.	Integrated Microcircuits Inc. Hopkins, MN	No Response
80.	International Sensor Systems Aurora, NB	No Response
81.	ITT Microsystems Deerfield Beach, FL	Received Data
82.	Leach Corporation Buena Park, CA	No Resopnse
83.	Narda Microwave Corporation Melville, NY	No Response
84.	Natel Engineering Co., Inc. Canoga Park, CA	No Response
85.	National Appliance Co. Portland, OR	No Response

86.	Parlex Methean, MA	No Response
87.	Teledyne Crystalonics Cambridge, MA	Received Data
88.	Transistor Specialties Inc. Danvers, MA	No Response
89.	TRW Inc. Lawndale, CA	No Response
90.	Watkin-Jonson Palo Alto, CA	Negative Reply
91.	LSI Logic Milpitas, CA	Will Not Send Data
92.	Rockwell International Dallas, TX	Negative Reply
93.	Micro Power Systems Santa Clara, CA	No Response
94.	W.G. Holt Company Irvine, CA	Negative Reply
95.	Veeco Instrument, Inc. Mellville, NY	No Response
96.	Universal Instrument Co. Binghamton, NY	No Response
97.	Oak Industries Crystal Lake, IL	No Response
98.	Methode Electronics Inc. Chicago, IL	No Response
99.	Digital Component Corporation Linden, NJ	No Response
100.	Elect Instruments, Inc. Daytona Beach, CA	No Response
101.	Garrett MFG. Co. Rexdale, Ontario Canada	No Response
102.	GTE Products Corporation Stamford, CT	No Response

103. Thick Film Int'l   No Response
   Indian Head, MD

104. Algorex Corporation   No Response
   Syosset, NY

105. Alpha Industries   No Response
   Colmar, PA

106. American Microsignal Corporation No Response
   Stanton, CA

107. Cermetek Microelectronics   No Response
   Sunnyvale, CA

108. CTS Corporation   No Response
   Elkhart, IN

109. Hytek Microsystems   No Response
   Los Gatos, CA

110. International MFG Svc's, Inc.   No Response
   Portsmouth, RI

111. Kyocera Int'l, Inc.   No Response
   San Diego, CA

112. Sparton Electronics   No Response
   Jackson, MI

113. Perforated Products, Inc.   No Response
   Brookline, MA

114. Trak Microwave   No Response
   Tampa, FL

115. Hycomp Inc.   Received Data
   Maynard, MA

116. Film Microelectronics   No Response
   Burlington, MA

117. Environmental Communications, Inc. No Response
   Costa Mesa, CA

118. Meret Inc.   No Response
   Santa Monica, CA

119. Statek Corporation   No Response
   Orange, CA

120. RHG Electronics Lab, Inc. Deer Park, NY	No Response
121. Fairchild MT. View, CA	No Response
122. Hewlett Packard Palo Alto, CA	Negative (No Data)
123. Hewlett Packard Santa Rosa, CA	Negative Custom Built
124. Hybrid Systems Billerica, MA	Promised Data
125. Datel-Intersil Mansfield, MA	Received Data
126. Master Logic Sunnyvale, CA	No Response
127. International Microcircuits Santa Clara, CA	No Response
128. Honeywell Deer Valley Park, AZ	No Response
129. Electrospace Systems, Inc. Richardson, TX	No Response
130. CTS Halex Irvine, CA	No Response
131. CTS of Berne, Inc. Berne, IN	No Response
132. Applied Microcircuits Cupertino, CA	Negative Reply
133. Teleydyne MEC Palo Alto, CA	No Response (Mircrowave Hybrid)
134. Ter Wave New Hyde Park, NY	No Response (Mircrowave Hybrid)
135. Struther Electronic Corporation Farmingdale, NY	No Response (Mircrowave Hybrid)
136. Optimax Div/Alpha Industries Colmar, PA	No Response (Mircrowave Hybrid)

137.	Microphase Corporation Cos Cob, CT	No Response (Mircrowave Hybrid)
138.	Hítachi America Arlington Heights, IL	No Response (Mircrowave Hybrid)
139.	General Dynamics San Diego, CA	No Response (Mircrowave Hybrid)
140.	Daico Industries Compton, CA	No Response (Mircrowave Hybrid)
141.	Cubic Corporation Oceanside, CA	No Response (Mircrowave Hybrid)
142.	Cincinnati Electronics Corporation Cincinnati, OH	No Response (Mircrowave Hybrid)
143.	BH Electronics Inc. Saint Paul, MN	No Response (Mircrowave Hybrid)
144.	Anaren Microwave, Inc. Syracuse, NY	No Response (Mircrowave Hybrid)
145.	American Electronics Lab Landsdale, PA	No Response (Mircrowave Hybrid)
146.	Trak Microwave Tampa, FL	No Response (Mircrowave Hybrid)
147.	Siemens South Iselin, NJ	No Response (Mircrowave Hybrid)
148.	GTE Sylvania Williamsport, PA	No Response (Mircrowave Hybrid)
149.	Goodyear Aerospace Corporation Akron, OH	No Response (Mircrowave Hybrid)
150.	Litton Industries Van Nuys, CA	No Response (Mircrowave Hybrid)
151.	Motorola, Inc. Austin, TX	Received Data
152.	Solitron Devices San Diego, CA	No Response Hybrid/VLSI
153.	Solitron Devices Riviera Beach, FL	No Response Hybrid/VLSI

154.	ITT North Electric Gallion, OH	No Response Hybrid/VLSI
155.	Varian Beverly, MA	No Response Hybrid/VLSI
156.	Itek Newton, MA	No Response Hybrid/VLSI
157.	Teledyne Microelectronics Los Angeles, CA	No Response Hybrid/VLSI
158.	Sprague Electric North Adams, MA	No Response Hybrid
159.	Isotronics New Bedford, MA	No Response Hybrid
160.	Analog Devices Wilmington, MA	Received Data Hybrid
161.	Unitrode Watertown, MA	Negative Data
162.	CTS Microelectronics West Lafayette, IN	Promised Data Hybrid Crystals
163.	Thinco Div Hull Corporation Hatboro, PA	Negative (No Data Available) Hybrid/VLSI
164.	Sandia Test Labs Albuquerque, NM	Promised Data
165.	HF&O Motorola Products Div. Phoenix, AZ	No Response Hybrid
166.	Amperex Electronic Corporation Slatersvile, RI	Negative Reply
167.	Dale Electronics Columbus, NE	Promised Data
168.	CTS Knights, Inc. Sandwich, IL	Promised Data
169.	Raytheon Andover, MA	Sent Data
170.	Bendix Baltimore, MD	Promised Data Hybrid/VLSI

154.	ITT North Electric Gallion, OH	No Response Hybrid/VLSI
155.	Varian Beverly, MA	No Response Hybrid/VLSI
156.	Itek Newton, MA	No Response Hybrid/VLSI
157.	Teledyne Microelectronics Los Angeles, CA	No Response Hybrid/VLSI
158.	Sprague Electric North Adams, MA	No Response Hybrid
159.	Isotronics New Bedford, MA	No Response Hybrid
160.	Analog Devices Wilmington, MA	Received Data Hybrid
161.	Unitrode Watertown, MA	Negative Data
162.	CTS Microelectronics West Lafayette, IN	Promised Data Hybrid Crystals
163.	Thinco Div Hull Corporation Hatboro, PA	Negative (No Data Available) Hybrid/VLSI
164.	Sandia Test Labs Albuquerque, NM	Promised Data
165.	HF&O Motorola Products Div. Phoenix, AZ	No Response Hybrid
166.	Amperex Electronic Corporation Slatersvile, RI	Negative Reply
167.	Dale Electronics Columbus, NE	Promised Data
168.	CTS Knights, Inc. Sandwich, IL	Promised Data
169.	Raytheon Andover, MA	Sent Data
170.	Bendix Baltimore, MD	Promised Data Hybrid/VLSI

171.	Westinghouse Baltimore, MD	Negative Reply Hybrid/VLSI
172.	TRW Electronic Group Orlando, FL	No Response
173.	Intel Chandler, AZ	Received Data
174.	Martin Marietta Aerospace Orlando, FL	Will not send data
175.	Honeywell Clearwater, FL	Will not send data

Appendix D:

VHSIC Reliability Survey Organization List

1. University of Illinois
    Computer System Group
    Coordinated Science Laboratory
    Urbana, IL

2. Raytheon Co.
    Missile Systems Div.
    Bedford, MA

3. Cornell University
    National Research & Resource
       Facility for Submicron Structures
    Ithaca, NY

4. Hughes Aircraft Company
    Electro-Optical & Data Systems Group
    Culver City, CA

5. TRW, Inc.
    Defense & Space Systems Group
    Redondo Beach, CA

6. AVCO Research Laboratory
    Everett, MA

7. University of Southern California
    Dept. of Electrical Engineering
    Los Angeles, CA

8. Stanford Research Institute
    Menlo Park, CA

9. Vela Associates
    Bethesda, MD

10. Honeywell, Inc.
    Systems & Research Center
    Minneapolis, MN

11. Sanders Associates, Inc.
    Federal Systems Group
    Nashua, NH

12. Hughes Aircraft Company
    Electro Optical & Data Systems Group
    El Segundo, CA

13. Westinghouse Electric Corporation
    Baltimore, MD

14. Raytheon Company
    Bedford Laboratories
    Bedford, MA

15. Research Triangle Institute
    Research Triangle Park, NC

16. IBM - Federal Systems Div.
    Manassas, VA

17. Sandia Laboratories
    Albuquerque, NM

18. Varian Extrion Division
    Gloucester, MA

19. Electron Beam Corp.
    San Diego, CA

20. Perkin Elmer
    Electro-Optical Division
    Norwalk, CT

21. General Electric
    Syracuse, NY

22. Lockheed California Co.
    Burbank, CA

23. Honeywell, Inc.
    Solid State Electronics Div.
    Plymouth, MN   55441

24. Texas Instruments, Inc.
    Dallas, TX

25. Hughes Research Laboratories
    Malibu, CA

26. University of Arizona
    Dept. of Electrical Engineering
    Tucson, AZ

27. Hewlett Packard
    Solid State Laboratory
    Palo Alto, CA

28. American Science & Engineering
    Arlington, MA

29. Palisades' Institute for Research
    Services, Inc.
    New York, NY

30. Rockwell International
    Anaheim, CA

31. Mellon Institute of Research
    Computer Engineering Center
    Pittsburgh, PA

32. California Technical Institute
    Jet Propulsion Labs
    Pasadena, CA

33. The Analytic Sciences Corp.
    Arlington, VA

34. General Electric
    Aerospace Electronic Systems Dept.
    Utica, NY

35. Boeing Aerospace Company
    Seattle, WA

36. Lockheed California Company
    Burbank, CA   91570

37. Honeywell Research Laboratory
    Bloomington, MN

38. Naval Ocean Systems Center
    San Diego, CA

39. Naval Surface Weapons Center
    White Oak, MD

40. AFWAL
    Wright-Patterson AFB, OH

41. Naval Weapons Center
    China Lake, CA

42. Rome Air Development Center
    Hanscom AFB, MA

43. OUSDR&E
    Washington, DC

44. Naval Air Systems Command
    Washington, DC

45. Naval Electronics Systems Command
    Washington, DC

46. U.S. Army Electronics Technology
     Devices Laboratory (ERADCOM)
    Fort Monmouth, NJ

47. Naval Air Development Center
    Warminister, PA

48. Naval Research Laboratory
    Washington, DC

49. Naval Avionics Center
    Indianapolis, IN

50. National Bureau of Standards
    Washington, DC

51. Naval Sea Systems Command
    Washington, DC

52. Naval Surface Weapons Center
    Dahlgren, VA

53. Department of the Navy
    Office of Naval Research
    Pasadena, CA

54. U.S. Army Missile Command
    Redstone Arsenal, AL

55. National Semiconductor
    Santa Clara, CA

56. Purdue University
    Computer Sciences Division
    Lafayette, IN

57. Motorola Semiconductor Products
    Phoenix, AZ

58. Arizona University
    Engineering Experiment Station
    Tucson, AZ

59. Stanford University
    Computer Systems Laboratory
    Stanford, CA

60. Palisades Institute for Research
        Services, Inc.
    Rosslyn, VA

61. U.S. Army Research Office
    Research Triangle Park, NC
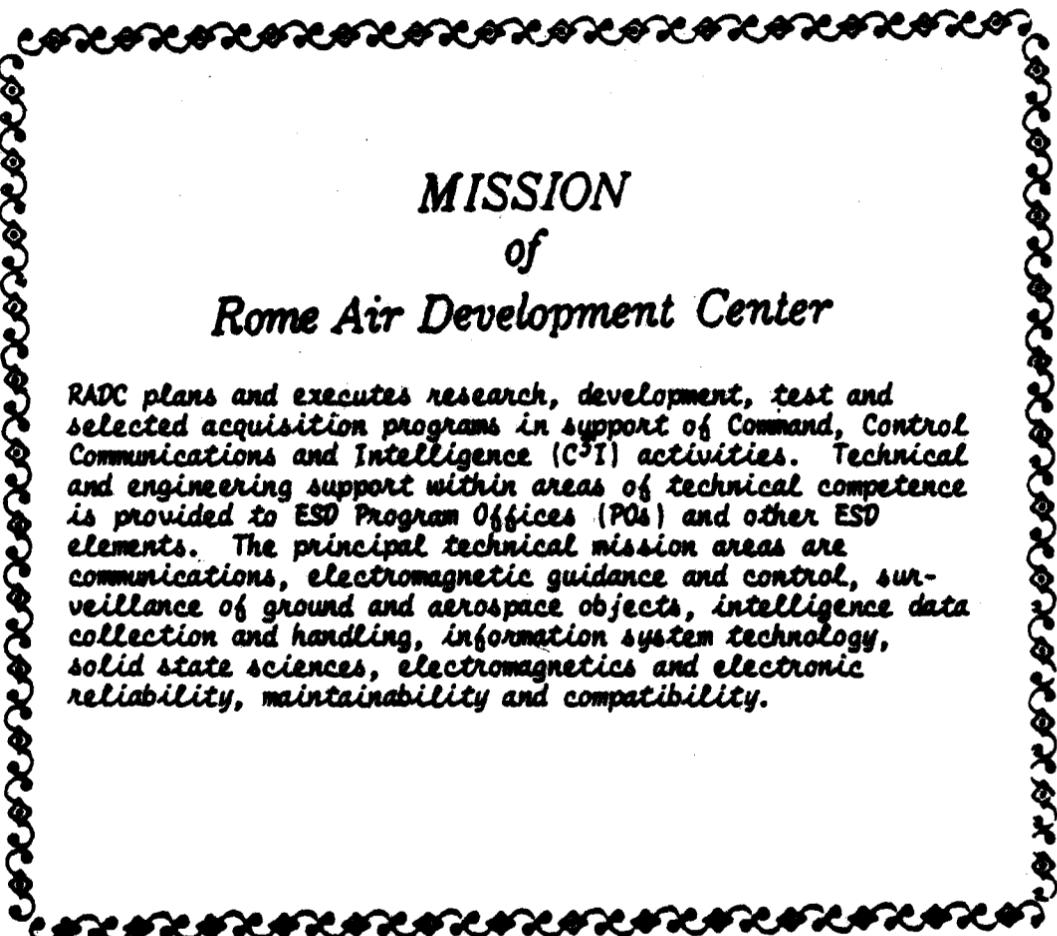
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RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, solid state sciences, electromagnetics and electronic reliability, maintainability and compatibility.

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